4645

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Date 9/23/02 Serial # 09/849,539 Priority Application Date 5/7/01

Your Name M. Lewis Examiner # _____

AU 2889 Phone 305-3743 Room Plaza B-3B09

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC s archer normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

09-24-02A09:33 PAID

Where have you searched so far on this case?
Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ✓ Nonpatent Literature ___ Other _____
Secondary Refs ✓ Foreign Patents ___
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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 3-13, 16, 17 + 38-68
I would like to do a follow up search. The applicant has amended + added claims.
Problem: Page 2 Paragraph 5-9
" 3 " 10
Solution: " " " 11-13
" 4 " 14+15
Derrick did the first search.

Staff Use Only	Type of Search	Vendors
Searcher: Derrick Hollock	Structure (#):	STN ✓
Searcher Phone: 306-0623	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation	Questel/Orbit
Date Searcher Picked Up: 9/24/02	Fulltext	Lexis-Nexis
Date Completed: 9/26/02	Patent Family	WWW/Internet
Searcher Prep/Rev Time: 120	Other	Other
Online Time: 79		

```
SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2002/Sep W5
         (c) 2002 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   6:NTIS  1964-2002/Sep W5
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*File   6: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File   8:Ei Compendex(R)  1970-2002/Sep W4
         (c) 2002 Engineering Info. Inc.
*File   8: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File  34:SciSearch(R) Cited Ref Sci  1990-2002/Sep W5
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*File  34: Alert feature enhanced for multiple files, duplicates
removal, customized scheduling. See HELP ALERT.
  File 434:SciSearch(R) Cited Ref Sci  1974-1989/Dec
         (c) 1998 Inst for Sci Info
  File  35:Dissertation Abs Online  1861-2002/Aug
         (c) 2002 ProQuest Info&Learning
  File  65:Inside Conferences  1993-2002/Sep W4
         (c) 2002 BLDSC all rts. reserv.
  File  77:Conference Papers Index  1973-2002/Sep
         (c) 2002 Cambridge Sci Abs
*File  77: As of October 1, 2002,Conference Papers Index will no longer
be available. See HELP CSA77 for a list of alternative files.
  File  94:JICST-EPlus  1985-2002/Jul W4
         (c)2002 Japan Science and Tech Corp(JST)
*File  94: There is no data missing. UDs have been adjusted to reflect
 the current months data. See Help News94 for details.
  File  99:Wilson Appl. Sci & Tech Abs  1983-2002/Aug
         (c) 2002 The HW Wilson Co.
  File 108:AEROSPACE DATABASE  1962-2002/Aug
         (c) 2002 AIAA
*File 108: As of October 1, 2002,Aerospace Database will no longer be
available. See HELP CSA108 for a list of alternative files.
  File 144:Pascal  1973-2002/Sep W5
         (c) 2002 INIST/CNRS
  File 238:Abs. in New Tech & Eng.  1981-2002/Sep
         (c) 2002 Cambridge Scient. Abstr
*File 238: As of October 1, 2002,ANTE will no longer be available. See
HELP CSA238 for a list of alternative files.
  File 305:Analytical Abstracts  1980-2002/Sep W3
         (c) 2002 Royal Soc Chemistry
*File 305: Alert feature enhanced for multiple files, duplicate
removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2002/Aug
         (c) 2002 DECHEMA
  File  14:Mechanical Engineering Abs  1973-2002/Sep
         (c) 2002 Cambridge Sci Abs
*File  14: As of October 1,2002, Mechanical Engineering Abstracts will no
longer be available. See HELP CSA14 for a list of alternative files.
  File  32:METADEX(R)  1966-2002/Sep B2
         (c) 2002 Cambridge Scientific Abs
*File  32: As of October 1,2002, Metadex(r) will no longer be
```

available. See HELP CSA32 for a list of alternative files.
File 96:FLUIDEX 1972-2002/Sep
(c) 2002 Elsevier Science Ltd.
File 103:Energy SciTec 1974-2002/Sep B2
(c) 2002 Contains copyrighted material
*File 103: For access restrictions see Help Restrict.

Set	Items	Description
S1	11962	BALL()GRID? ? OR BALLGRID? OR BGA OR BGAS OR PBGAS OR PBGA OR CGA OR CGAS
S2	3064	(SOLDER OR SOLDERING OR SOLDERED OR BRAZ?)(2N)(BALL OR BALLS OR PADS OR PAD OR SPHERE? ?)
S3	290321	(HEAT? OR WARM? OR HOT? ? OR THERMOL? OR THERMAL? OR PREHEAT? OR MELT? OR FUSE? ? OR FUSING? ? OR FUSION?)(3N)(SPREAD? OR CIRCULATE? OR DISPERS? OR DISTRIBUT? OR RADIAT? OR SCATTER? OR COVER? OR OVERLAY?)
S4	22912	((HIGH?? OR HEIGHTEN? OR RAIS? OR INCREAS? OR ELEVAT?)(2N)(TEMP? ? OR TEMPERATUR?))(3N)(SPREAD? OR CIRCULATE? OR DISPERS? OR DISTRIBUT? OR RADIAT? OR SCATTER? OR COVER? OR OVERLAY?)
S5	67188	(CIRCUIT)(2N)(BOARD) OR SYSTEM()BOARD OR MOTHERBOARD OR PCB
S6	252632	SOLDER OR SOLDERING OR SOLDERED OR BRAZ?
S7	1845277	IC OR ICS OR ((INTEGRATED OR LOGIC)(W)(CIRCUIT? ?)) OR (MICRO)(W)(CIRCUIT? ? OR CHIP? ? OR ELECTRONIC?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ? OR LOGIC(W) CIRCUIT? ? OR WAFER? ? OR MICROELECTRONIC?
S8	5932	CC=B2220 Integrated circuits
S9	4045	(CONTACT? OR BONDING)(2N)(PAD OR PADS OR BUMP OR BUMPS)
S10	11941	(WIRE OR WIRES OR LINE OR LINES)(2N)(BOND?)
S11	319	(CONDUCTIV?)(3N)(BUMP? OR PAD OR PADS)
S12	7930227	ENCLOS??? OR HOUS??? OR CASE? ? OR CONTAIN? OR ENCASE? OR ENCAPSUL? OR PACKAG?
S13	7412	S1 AND S12
S14	213	S13 AND (S3 OR S4)
S15	9	S14 AND STIFFENER
S16	8	RD (unique items)
S17	53	S14 AND S2
S18	33	RD (unique items)
S19	30	S18 NOT S15
S20	33	S14 AND METAL? ?
S21	22	S20 NOT (S17 OR S15)
S22	13	RD (unique items)
S23	42	S14 AND (COPPER OR CU)
S24	18	S23 NOT (S17 OR S15 OR S20)
S25	13	RD (unique items)
S26	15	S14 AND (ALUMINUM OR ALUMINIUM OR AL)
S27	5	S26 NOT (S17 OR S15 OR S20 OR S23)
S28	1845792	S7 OR S8
S29	86	S28 AND STIFFENER
S30	7	S29 AND (S3 OR S4)
S31	0	S30 NOT (S17 OR S15 OR S20 OR S23 OR S26)
S32	6	S14 AND PLANAR
S33	0	S14 AND S11
S34	0	S32 NOT (S17 OR S15 OR S20 OR S23 OR S26 OR S30)

16/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6091405 INSPEC Abstract Number: B9901-0170J-029
Title: Performance and reliability of a cavity down tape **BGA package**
Author(s): Schueller, R.D.; Aeschliman, D.; Chiew, T.H.
Author Affiliation: 3M Electron. Products Div., Austin, TX, USA
Conference Title: Proceedings of the 1997 1st Electronic Packaging Technology Conference (Cat. No.97TH8307) p.151-62
Editor(s): Tay, A.A.O.; Beng, L.T.
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 319 pp.
ISBN: 0 7803 4157 0 Material Identity Number: XX98-02804
U.S. Copyright Clearance Center Code: 0 7803 4157 0/97/$10.00
Conference Title: Proceedings of the 1997 1st Electronic Packaging Technology Conference
Conference Sponsor: Inst. Mater. Res. & Eng.; Inst. Microelectron.; IEEE CPMT Soc
Conference Date: 8-10 Oct. 1997 Conference Location: Singapore
Language: English
Abstract: As the demand for greater I/O has increased, so has the interest in **ball grid** array **packaging** . It is well recognized in the **packaging** industry that as the pin counts increase above 208, **BGA packages** become more attractive due to their small form factor and ease of board attach. However, along with the general trend for higher I/O, an increasing percentage of ICs are also running at over 200 MHz and 4 W of power. These IC requirements surpass the capability of standard QFP and **PBGA packages**. To satisfy this demand, there has been a major push for high performance **BGA packages** which are considerably more cost effective than ceramic **package** alternatives. Tape **BGA packages** provide an excellent cost/performance solution in this market segment and are gaining a great deal of attention. With the fine line capability of flexible circuits (down to 25 mu m lines and spaces), the wire bond fingers can be moved very close to the die. This enables die shrinkage in pad limited die and reduces wire length, which is often the main source of **package** self inductance. Excellent thermal properties are achieved by directly attaching the die to a thermally conductive copper **stiffener** or **heat spreader**. The copper CTE also matches closely with that of the board to maximize thermal cycle reliability. This product can be provided at a competitive price due to the minimization of materials and a simplified production process. The result is a low cost, high performance **package** with excellent reliability. This paper discusses the electrical and thermal performance of this **package** along with the reliability.
Subfile: B

16/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6010654 INSPEC Abstract Number: B9810-0170J-038
Title: Tape **ball grid** array with ground plane

Author(s): Karnezos, M.
Author Affiliation: Signetics High Technol. Inc., San Jose, CA, USA
Conference Title: Area Array Packaging Technologies. Workshop on Flip Chip, CSP and Ball Grid Arrays p.111-24
Publisher: Fraunhofer Inst. Reliability & Microintegration, Berlin, Germany
Publication Date: 1997 Country of Publication: Germany 304 pp.
Material Identity Number: XX98-00095
Conference Title: Proceedings of Area Array Packaging Technologies Workshop on Flip Chip and Ball Grid Arrays
Conference Date: 17-19 Nov. 1997 Conference Location: Berlin, Germany
Language: English
Abstract: The Signetics-tape **ball grid** array (S-TBGA) is a cavity down **BGA** using a copper/polyimide flex interconnect substrate and a copper **heat spreader** assembly which serves as the ground plane and also as the tape carrier/**stiffener**. The flex substrate, with a pitch of 60 mu m, is capable of routing up to seven rows of solder balls at 1.27 mm pitch, allowing maximum ball count for a fixed body size. The minimum bond pitch on the **package** is limited to 110 mu m only by the wire bonding process capabilities, yet reduces wire lengths down to 1.5 mm to produce very low inductance signal connections. Direct reflow of solder balls on the ground plane and direct wire bonds from the die to the ground ring provide a very low inductance plane for all the ground connections. The combination of a single-metal tape with ground plane offers the high electrical performance of the two-metal tape, but at a fraction of the cost. The low **package** profile at 1.35 mm thickness and a **heat spreader** which **covers** the whole **package** surface provide a very effective EMI shield and reduce noise. The direct attachment of the die against the copper **heat spreader** provides for the lowest possible thermal resistance, carrying about 50% of the heat to the ambient. The remaining heat is conducted through the 0.15 mm thin tape and the numerous solder balls to the motherboard. The combination of the single-metal tape and the stamped **heat spreader**/ground plane assembly allow for a high performance **package** at low enough cost for high volume applications.
Subfile: B

16/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5704140 INSPEC Abstract Number: B9711-0170J-030
Title: Electrical design of a low cost and high performance plastic **ball grid** array **package**-NuBGA
Author(s): Tai-Yu-Chou; Wu, F.; Lau, J.; Kuan-Luen Chen
Author Affiliation: Express Package Syst. Inc., Palo Alto, CA, USA
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.1081-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE;

Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: This paper presents a new class of low cost, electrically and thermally optimized **ball grid** array **packages**, called NuBGA (new and useful **ball grid** array). The **package** is suitable for both low and high pin count applications. NuBGA is a cavity down **package** with a metal **heatspreader covering** the entire back surface of the **package**. **Heat spreader** is laminated with a single core double sided organic substrate. Optimized electrical performance is achieved using the design concepts of Split-Wrap-Around (SWA) and Split-Via-Connections (SVC). All traces on the core substrate can be designed into mu -stripline and co-planar stripline structures. Further enhanced thermal and electrical performance NuBGA can be achieved by applying an additional metal **stiffener** and thinner core substrate. In this paper, the presentation is focus on (1) the unique design concept, (2) the electrical analysis, (3) the electrical measurement, and (4) the performance comparison with standard **packages**.
Subfile: B

16/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5590831 INSPEC Abstract Number: B9707-0170J-025
Title: Thermal characterization of tape **ball grid** array **packages**
Author(s): Shaukatullah, H.; Andros, F.E.; Gaynes, M.A.; Loveland, C.P.
Author Affiliation: Microelectron. Div., IBM Corp., Endicott, NY, USA
Conference Title: Proceedings of the 1996 International Electronics Packaging Conference p.377-95
Publisher: Int. Electron. Packaging Soc, Edina, MN, USA
Publication Date: 1996 Country of Publication: USA 681 pp.
Material Identity Number: XX96-02693
Conference Title: Proceedings of International Electronics Packaging Society Conference. 1996 Annual Conference `A Powerhouse Program'
Conference Sponsor: Int. Electron. Packaging Soc
Conference Date: 29 Sept.-1 Oct. 1996 Conference Location: Austin, TX, USA
Language: English
Abstract: The surface mount tape **ball grid** array (TBGA) **package** consists of a flexible polyimide tape with copper circuitry on both sides, attached to a metal **stiffener** using an electrically insulating adhesive. The integrated chip is bonded to one side of the tape using thermocompression bonding or flip-chip solder balls. The other side of the tape has an array of solder balls for soldering the **package** to the card. Due to the metal **stiffener** and exposed back side of the chip, the TBGA **package** lends itself well to **thermal** enhancement. A metal **cover** plate can be directly bonded to the back side of chip and the **stiffener** to improve the thermal performance. For further thermal enhancement, heat sinks can be attached with thermally conductive adhesive to the cover plate. This paper describes the procedure used for thermal characterization of the TBGA **packages** with and without the **heat** sink and **cover** plate. **Thermal**

performance and thermal reliability test data are reviewed. The paper also discusses the effects of card size, card conductivity and the number of solder balls on the thermal performance.
Subfile: B

16/3,AB/5 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04792702
E.I. No: EIP97083790057
Title: Electrical design of a low cost and high performance plastic **ball grid** array **package** - NuBGA
Author: Chou, Tai-Yu; Wu, Frank; Lau, John; Chen, Kuan-Luen
Corporate Source: Express Package Systems, Inc, Palo Alto, CA, USA
Conference Title: Proceedings of the 1997 47th IEEE Electronic Components & Technology Conference
Conference Location: San Jose, CA, USA Conference Date: 19970518-19970521
E.I. Conference No.: 46865
Source: Proceedings - Electronic Components and Technology Conference 1997. IEEE, Piscataway, NJ, USA,97CB36048. p 1081-1086
Publication Year: 1997
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: This paper presents a new class of low cost, electrically and thermally optimized **ball grid** array **packages**, called NuBGA (new and useful **ball grid** array). The **package** is suitable for both low and high pin count applications. NuBGA is a cavity down **package** with a metal **heatspreader covering** the entire back surface of the **package**. **Heat spreader** is laminated with a single core double sided organic substrate. Optimized electrical performance is achieved using the design concepts of Split-Wrap-Around (SWA) and Split-Via-Connections (SVC). All traces on the core substrate can be designed into mu -stripline and co-planar stripline structures. Further enhanced thermal and electrical performance NuBGA can be achieved by applying an additional metal **stiffener** and thinner core substrate. In this paper, the presentation is focus on (1) the unique design concept, (2) the electrical analysis, (3) the electrical measurement, and (4) the performance comparison with standard **packages**. (Author abstract) 5 Refs.

16/3,AB/6 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03995291 JICST ACCESSION NUMBER: 99A0050220 FILE SEGMENT: JICST-E
High-performance and Low-cost Projectional **Stiffener** for TBGA.
OHTAKA O (1); OHMORI T (1); KAWANOBE T (1); IMAI N (1)
(1) Hitachi Cable, Ltd.
Hitachi Cable Rev, 1998, NO.17, PAGE.51-56, FIG.10, TBL.1, REF.3
JOURNAL NUMBER: Y0198AAI
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: English COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The TBGA (Tape **BGA**) **package** is one of the most r.emarkable **packages** available, especially when a high pin count and good thermal performance are required. The TBGA **package** consists of a TAB, a **stiffener**, and a **heat spreader**. The **stiffener** is the back-bone of the TBGA, providing the solder ball coplanarity needed for sticking on the TAB, and the **heat spreader** is needed for effective heat dissipation. The set price of **stiffener** and **heat spreader** is higher than the market target, there is the strong need for cost down of the set. We therefore developed a new **stiffener** in which the conventional **stiffener** and **heat spreader** are combined into by a press process. investigation of the TBGA with this new **stiffener** shows that its performance is at least as good as that of the conventional type of **stiffener**. (author abst.)

16/3,AB/7 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03396477 JICST ACCESSION NUMBER: 97A0693774 FILE SEGMENT: JICST-E
Semiconductor device.
KUROSU ATSUSHI (1)
(1) Toshiba Corp.
Toshiba Gijutsu Kokaishu, 1997, VOL.15,NO.44, PAGE.149-151, FIG.4
JOURNAL NUMBER: L0795AAY ISSN NO: 0288-2701
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: By unifying a **stiffener** and cover plate of an FC-**BGA** **package**, a substrate structure which could **radiate** a **heat** directly to an mounted substrate by contacting the cover plate to a chip, was developed. The cover plate is bonded to the upper surface of the chip and is formed so as to surround two or four facing sides of the **stiffener**.

16/3,AB/8 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02568352 JICST ACCESSION NUMBER: 95A0893293 FILE SEGMENT: JICST-E
TAB-**BGA** (COCB) **Package** for Next-Generation LSI **Packages**.
MITA M (1); KUMAKURA T (1)
(1) Hitachi Cable, Ltd.
Hitachi Cable Rev, 1995, NO.14, PAGE.45-52, FIG.14, TBL.2, REF.4
JOURNAL NUMBER: Y0198AAI
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

ABSTRACT: Consideration of TAB-**BGA** (COCB: Chip on Chip **Ball grid** array) had started from thinking of new VLSI **package** design revolution. This **package** is assembled by combining TAB (Tape Automated Bonding) and LEM (Low Melting point Au/Sn Eutectic Microsoldering) technology. Fine pitch interconnection between VLSI chip pads and TAB inner leads significantly reduces LSI chip dimensions and **package** body size. Numerous VLSI's I/O pins are lead to routing of interposer and **stiffener** having spherical balls on it's bottom surface. LEM is a new microjoining technique for LSI **package** assembly. This technology doesnt damage organic materials, such as FR-5 or BT resin, and others used for interposers and substrates. This makes it possible to reduce the **package** cost by offering an alternative to ceramic **packages**. Satisfactory electrical performance and a thermal sinking effect are obtained by combining a small body design and **heat spreader** attachments. (author abst.)

19/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7352023 INSPEC Abstract Number: B2002-09-0170J-100
Title: Thermomechanical reliability of underfilled **BGA packages**
Author(s): Pyland, J.; Pucha, R.V.; Sitararnan, S.K.
Author Affiliation: George W. Woodruff Sch. of Mech. Eng., Georgia Inst. of Technol., Atlanta, GA, USA
Journal: IEEE Transactions on Electronics Packaging Manufacturing vol.25, no.2 p.100-6
Publisher: IEEE,
Publication Date: April 2002 Country of Publication: USA
CODEN: ITEPFL ISSN: 1521-334X
SICI: 1521-334X(200204)25:2L.100:TRUP;1-G
Material Identity Number: H313-2002-003
U.S. Copyright Clearance Center Code: 1521-334X/02/$10.00
Language: English
Abstract: The effect of underfill on various thermomechanical reliability issues in super **ball grid** array (SBGA) **packages** is studied in this paper. Nonlinear finite element models with underfill and no underfill are developed taking into consideration the process-induced residual stresses. In this study, the solder is modeled as time and temperature-dependent, while other materials are modeled temperature and direction-dependent, as appropriate. The stress/strain variations in the **package** due to thermal cycling are analyzed. The effect of underfill is studied with respect to magnitude and location of time-independent plastic strain, time-dependent creep strain and total inelastic strain in **solder balls**. The effect of copper core on the **solder ball** strains is presented. The possibility of delamination at the interposer-underfill interface as well as substrate-underfill interface is studied with the help of qualitative interfacial stress analysis. Results on SBGA **packages** indicate that the underfill does not always enhance **BGA** reliability, and that the properties of the underfill have a significant role in the overall reliability of the **BGA packages**. The predicted number of thermal cycles to solder joint fatigue are compared with the existing experimental data on similar nonunderfilled **BGA packages**.
Subfile: B

19/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7140911 INSPEC Abstract Number: B2002-02-0170J-015
Title: Reliability study of a high-pin-count fine-pitch flip-chip **ball grid** array
Author(s): Yuan Li; Xie, J.; Verma, T.
Author Affiliation: Altera Corp., San Jose, CA, USA
Journal: International Journal of Microelectronic Packaging, Materials and Technologies vol.1, no.4 p.269-76
Publisher: Gordon & Breach,
Publication Date: 2001 Country of Publication: Switzerland

CODEN: IJMTF3 ISSN: 1023-6228
SICI: 1023-6228(2001)1:4L.269:RSHC;1-E
Material Identity Number: F175-2001-001
Language: English
Abstract: To provide higher I/O density and better electrical and thermal performance, a 1.0-mm-pitch flip-chip GA was developed. Currently, the **solder ball** count, the die size and the **package** size vary between 600 and 1100, 15 mm 25 mm, and 27 mm to 33 mm respectively. In addition to thermal cycling tests, finite element analysis has been used as an important tool to study reliability of this **package**. In the initial stage of **package** development, two substrate materials, BT and high-CTE (coefficient of thermal expansion) ceramic, were compared. After the substrate was determined, a design of experiment (DOE) was set up to systematically study the effect of the dimensions and properties of underfill and **heat spreader** . The findings of this DOE study have provided us important guidelines to improve reliability of this **package**.
Subfile: B

19/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

7131159 INSPEC Abstract Number: B2002-02-0170J-007
Title: Thermal characterization of tape **BGA package** by modeling
Author(s): Han Jiang-Bo
Author Affiliation: Semicond. Product Group, Agilent Technols., Singapore, Singapore
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.4229 p.202-8
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 2000 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(2000)4229L.202:TCTP;1-P
Material Identity Number: C574-2001-083
U.S. Copyright Clearance Center Code: 0277-786X/00/$15.00
Conference Title: Microelectronic Yield, Reliability, and Advanced Packaging
Conference Sponsor: SPIE: Nanyang Technol. Univ
Conference Date: 28-30 Nov. 2000 Conference Location: Singapore
Language: English
Abstract: In microelectronic industry, numerical modeling is an effective way to predict thermal performance of IC **packages** in the initial development stage. Moreover, thermal simulation can provide a greater understanding of the physics of the problem, allowing design to be optimized quickly and cheaply, thereby shortening **packaging** development cycle time and keeping expensive experimental measurements to a minimum. In this study, 3D finite element analysis (FEA) thermal models capturing the details of the **solder ball** and internal structure of the tape **BGA package** are developed. Accuracy of the developed FEA models is validated by bench marking with the measurement for 35mm by 35mm 352 TBGA **package** . Numerical results of the thermal performance of the TBGA **package** under various die size and **heat**

-**spreader** remaining thickness are presented. The thermal metrics, Theta-JA, Psi-JT, and Psi-JB, of the **package** are characterized numerically. Relationships between these three thermal metrics are established. These relationships are useful to correlate one thermal parameter of the **package** to another.
Subfile: B

19/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6777136 INSPEC Abstract Number: B2001-01-0170J-059
Title: Fundamentals of **BGA** ball attach reflow process
Author(s): Ko, M.
Author Affiliation: Res. Int., Eden Prairie, MN, USA
Conference Title: Pan Pacific Microelectronics Symposium. Proceedings of the Technical Program p.194-9
Publisher: Surface Mount Technol. Assoc, Edina, MN, USA
Publication Date: 2000 Country of Publication: USA 423 pp.
Material Identity Number: XX-2000-01481
Conference Title: Proceedings of Fifth Annual Pan Pacific Microelectronics Symposium
Conference Sponsor: GPD
Conference Date: 25-27 Jan. 2000 Conference Location: Maui, HI, USA
Language: English
Abstract: The fundamentals of **solder ball** reflow for the **BGA** ball attach process are discussed. The content is divided into three sections: heat transfer modes, reflow oven convection technologies, and temperature profile mechanics. There are three basic heat transfer modes: conduction, convection and radiation. For most reflow ovens, forced convection is the dominant heat transfer mode. Understanding heat transfer modes assists process engineers in reflow application troubleshooting. In reflow ovens, there are two basic methods of achieving forced convection: fans and pressure sources. Typically, fans are used to achieve convection and recirculate process gas. Examples of pressure sources are compressors and nitrogen tanks. The benefits of both methods are discussed. In convection heat transfer, the gas temperature and speed provide quantitatively different effects in product heating. Adjusting the process gas/product temperature difference is a more effective method of heat transfer control. In general, higher gas speed or volumetric flow rate improves temperature uniformity across products. There are four different elements in reflow profiling: preheat, dryout, reflow and cooling. There is a definite procedure in performing temperature profiling. Understanding the relationship between heater set point temperatures, desired profile temperature, gas speed and conveyor speed allows one to achieve the desired temperature profiles with improved efficiency and accuracy. Understanding and practicing the reflow process fundamentals for **BGA packaging** can enhance the productivity and lower operational cost.
Subfile: B

19/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6724574 INSPEC Abstract Number: B2000-11-0170J-082, C2000-11-7410D-132
Title: An investigation of thermal enhancement on flip chip plastic **BGA packages** using CFD tool
Author(s): Lee, T.-Y.
Author Affiliation: Interconnect Syst. Labs., Motorola Inc., Tempe, AZ, USA
Journal: IEEE Transactions on Components and Packaging Technologies vol.23, no.3 p.481-9
Publisher: IEEE,
Publication Date: Sept. 2000 Country of Publication: USA
CODEN: ITCPFB ISSN: 1521-3331
SICI: 1521-3331(200009)23:3L.481:ITEF;1-1
Material Identity Number: H324-2000-004
U.S. Copyright Clearance Center Code: 1521-3331/2000/$10.00
Language: English
Abstract: This paper demonstrates the advantage of applying Predictive Engineering in the thermal assessment of a 279 inputs/outputs (I/Os), six-layer, depopulated array flip chip **PBGA package**. Thermal simulation was conducted using a computational fluid dynamics (CFD) tool to analyze the heat transfer and fluid flow in a free convection environment. This study first describes the modeling techniques on a multilayer substrate, thermal vias, solder bumps, and printed circuit board (PCB). For a flip chip **package** without any thermal enhancement, more than 90% of the total power was conducted from the front surface of the die through the **solder ball** interconnects to the substrate, then to the board. To enhance the thermal performance of the **package**, the heat transfer area from the backside of the die needs to increase dramatically. Several thermal enhancing techniques were examined. These methods included a copper **heat spreader** with various thicknesses and with thermal pads, metallic lid, overmolded with and without a **heat spreader**, and with **heat** sink. An aluminum lid and a heat sink gave the best improvement; followed by a **heat spreader** with **thermal** pads. Both methods reduced thermal resistance by an average of 50%. Detailed analyses on heat flow projections are discussed.
Subfile: B C

19/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6635959 INSPEC Abstract Number: B2000-08-0170J-078, C2000-08-7410D-058
Title: Thermal characterization of cavity-down TBGA **package** with Flotherm simulation
Author(s): Eric Cho; Eric Tan; Yur-Tsai Lin
Author Affiliation: Flotrend Co., Taipei, Taiwan
Conference Title: Sixteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.00CH37068) p.68-75
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA xi+298 pp.
ISBN: 0 7803 5916 X Material Identity Number: XX-2000-00788
U.S. Copyright Clearance Center Code: 0 7803 5916 X/2000/$10.00
Conference Title: Sixteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium. Proceedings 2000
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc

Conference Date: 21-23 March 2000 Conference Location: San Jose, CA, USA
Language: English
Abstract: This paper presents the use of the finite volume analysis method in predicting thermal performance of a TBGA (Tape **Ball Grid** Array) **package** in a **package** level and in a board level, respectively. The effect of **heat spreader** thickness is also analyzed and the results show that the larger the thickness, the lower the junction temperature. However, it is also shown that more than 75% of heat dissipation is conducted away through **solder balls** rather than the **heat spreader**. The **thermal** performance of a TBGA **package** mounted on a real graphic card is next analyzed in the board level and the results are compared with two **PBGA packages**. With other heat sources around the **package** on the graphic card, the corresponding junction temperatures increase dramatically. The thermal performance of the TBGA is superior to that of both **PBGAs**. The results also show that a heat sink module attached on the top of the **package** can further improve the thermal performance of the TBGA **package**.
Subfile: B C

19/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6493755 INSPEC Abstract Number: B2000-03-0170J-170
Title: Effect of **heat-spreader** sizes on the **thermal** performance of large cavity-down plastic **ball grid** array **packages**
Author(s): Lau, J.; Chen, T.; Lee, S.-W.R.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Transactions of the ASME. Journal of Electronic Packaging vol.121, no.4 p.242-8
Publisher: ASME,
Publication Date: Dec. 1999 Country of Publication: USA
CODEN: JEPAE4 ISSN: 1043-7398
SICI: 1043-7398(199912)121:4L.242:EHSS;1-5
Material Identity Number: N602-2000-001
Language: English
Abstract: The effect of **heat-spreader** size on the temperature **distribution, thermal** resistance, and cooling power of a set of cost-effective cavity-down plastic **ball grid** array (**PBGA**) **packages** assembled on a FR-4 epoxy glass printed circuit board (PCB) is presented. The sizes of these **packages** are 35*35 mm and 40*40 mm, with 4 and 5 rows of **solder balls**.
Subfile: B

19/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

6369501 INSPEC Abstract Number: B1999-11-0170J-083
Title: Thermal fatigue reliability of cavity-down **BGA** assemblies

Author(s): Pao, Y.-H.; Song, X.; Jih, E.; Adams, R.
Author Affiliation: Res. Lab., Ford Motor Co., Dearborn, MI, USA
Conference Title: Proceedings of the Technical Program. NEPCON East 97. Conference p.195-8
Publisher: Reed Exhibition, Norwalk, CT, USA
Publication Date: 1997 Country of Publication: USA 362 pp.
Material Identity Number: XX-1997-01717
Conference Title: Proceedings of NEPCON East
Conference Date: 9-12 June 1997 Conference Location: Boston, MA, USA
Language: English
Abstract: The finite element analysis of a typical cavity-down **BGA package** identifies potential reliability problems that are different from the conventional cavity-up **PBGA packages**. Most issues identified are related to the local warpage of die/**heat spreader** , which results in high and additional stresses in die, die attachment, **heat spreader**, and **solder balls**. Design changes are needed to reduce the local warpage. The predicted reliability of **solder balls** seem to outperform those of the conventional **PBGA solder balls**, primarily because of a better match of coefficient of thermal expansion between the FR-4 substrate and the **package** and the arrangement of die and **solder balls**. The critical **solder balls** are identified to be those located in the middle ring along the center fine of the **package**. The arrangement of the **solder balls** and the utilization of solder mask result in high hydrostatic stresses in the **solder/pad** interfaces and may lead to interfacial failure of the **packages** . Reduction in the stiffness of solder mask may alleviate the constraint on the interfaces and in turn decrease the hydrostatic stresses.
Subfile: B

19/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

6319767 INSPEC Abstract Number: B1999-09-0170J-103, C1999-09-7410D-083
Title: Optimizing cost and thermal performance: rapid prototyping of a high pin count cavity-up enhanced plastic **ball grid** array (EPBGA) **package**
Author(s): Zahn, B.A.
Author Affiliation: Package Characterization Lab., ChipPAC Inc., Chandler, AZ, USA
Conference Title: Fifteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.99CH36306) p.133-41
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA xvi+299 pp.
ISBN: 0 7803 5264 5 Material Identity Number: XX-1999-01041
U.S. Copyright Clearance Center Code: 0 7803 5264 5/99/$10.00
Conference Title: Fifteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium. SEMI-THERM. Proceedings 1999
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc
Conference Date: 9-11 March 1999 Conference Location: San Diego, CA, USA
Language: English
Abstract: A three-dimensional finite element model of a 420 lead (5 row perimeter) cavity-up enhanced plastic **ball grid** array (EPBGA)

package was developed using the ANSYS/sup TM/ finite element simulation code. The developed model was utilized to perform a sensitivity analysis in order to quantify the effects of varying **package** and system motherboard designs. Design variables included: (1) chip size; (2) **package** substrate metallized plane layers; (3) motherboard metallized plane layers; (4) inner **solder ball** matrix and vias; (5) **package** aluminum **heat spreader** thickness; and (6) chip power dissipation. Predicted **package** junction-to-ambient thermal resistance (theta /sub JA/) values were used in conjunction with a central composite design of experiments to develop a response surface equation which quickly predicts EPBGA **package** thermal performance as a function of the six design variables. The methodology described allows for rapid analysis of design options in the "dynamic" environment of prototyping, and the implementation of optimized cost effective **package** designs to meet required standards under multiple customer environments.
Subfile: B C

19/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

6271398 INSPEC Abstract Number: B1999-07-0170J-191
Title: Effect of **heat-spreader** sizes on the **thermal** performance of large cavity-down plastic **ball grid** array **packages**-NuBGA
Author(s): Lau, J.; Chen, T.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Microelectronics International vol.16, no.2 p.24-33
Publisher: MCB University Press,
Publication Date: April 1999 Country of Publication: UK
CODEN: MIINF2 ISSN: 1356-5362
SICI: 1356-5362(199904)16:2L.24:EHSS;1-E
Material Identity Number: D084-1999-002
Language: English
Abstract: The effect of **heat-spreader** size on the temperature **distribution**, **thermal** resistance, and cooling power of a set of cost-effective cavity-down plastic **ball grid** array (**PBGA**) **packages** , NuBGA, assembled on an FR-4 epoxy glass printed circuit board (PCB) is presented, from the results of a finite element analysis study. The sizes of these **packages** are 35*35 mm and 40*40 mm and with four and five rows of **solder balls**.
Subfile: B

19/3,AB/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC

6128186 INSPEC Abstract Number: B1999-02-0170J-088
Title: S-TBGA: A cost effective alternative to enhanced **PBGAs**
Author(s): Karnezos, M.
Author Affiliation: Signetics KP, San Jose, CA, USA
Conference Title: Proceedings of the Technical Program. NEPCON West '98.

Conference Part vol.3 p.1412-23 vol.3
Publisher: Reed Exhibition, Norwalk, CT, USA
Publication Date: 1998 Country of Publication: USA 3 vol. 1546 pp.
Material Identity Number: XX-1998-02004
Conference Title: Proceedings of NEPCON West 98
Conference Date: 1-5 March 1998 Conference Location: Anaheim, CA, USA
Language: English
Abstract: S-TBGA is a cavity down **BGA** that provides superior power dissipation and equivalent electrical performance compared to a four-layer enhanced **PBGA** at competitive cost. It uses a thin flex interconnect substrate with one metal layer and an integral **heat spreader** with ground plane. The die is attached to the **heat spreader**, the ground pads are wire bonded to the cavity ground ring, and the ground **solder balls** are reflowed directly on the ground plane. This low inductance plane is used for all ground connections and carries all ground currents. All signal and power connections are via the flex substrate. The low **package** profile at 1.35 mm thick and the **heat spreader** which **covers** the whole **package** surface provide an effective EMI shield and reduce noise. The combination of single-metal tape with ground plane offers the high electrical performance of a two-metal tape at a fraction of the cost. Direct die attachment to a Cu **heat spreader** provides the lowest **thermal** resistance, carrying about 50% of the heat to ambient. The remaining heat is conducted through the 0.15 mm thin substrate and the **solder balls** to the motherboard. The 60 mu m high density routing of the substrate allows routing of up to seven rows of **solder balls** in a single metal layer with finest usable bond finger pitch of 100 mu m, short wires <1.2 mm, large maximum die size and no minimum die size specification. The combination of single-metal tape and stamped **heat spreader** /ground plane assembly allow for a high performance **package** at low cost for high volume applications. Special design features, **package** structure and assembly process are discussed and performance data are given.
Subfile: B

19/3,AB/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC

6049268 INSPEC Abstract Number: B9811-0170J-056
Title: Manufacturing process for combination lead frame/TAB **BGA**
Author(s): Mita, M.; Murakami, G.; Kumakura, T.; Kashiwabara, F.
Author Affiliation: Densen Works, Hitachi Cable Ltd., Ibaraki, Japan
Journal: IEEE Transactions on Components, Packaging & Manufacturing Technology, Part C (Manufacturing) vol.21, no.3 p.204-10
Publisher: IEEE,
Publication Date: July 1998 Country of Publication: USA
CODEN: ITCMF2 ISSN: 1083-4400
SICI: 1083-4400(199807)21:3L.204:MPCL;1-U
Material Identity Number: D485-98004
U.S. Copyright Clearance Center Code: 1083-4400/98/$10.00
Language: English
Abstract: The combination lead frame/tape automated bonding **ball grid** array (TAB **BGA**) has been studied to improve the manufacturability of thin **ball grid** array (TBGA) large scale

integrated (LSI) **packages** . Ordinary lead frames and the TAB tape carriers have been applied to make the assembly of TBGA easier. The base technologies, the materials of the lead frame, and the TAB tape were thoroughly applied to the **heat spreader** and the fine routing flexible substrate. The lead frames as the **heat spreader** and the tape (manufactured by the line of the TAB tape for wire bonding substrate) are combined with a high thermal resistive adhesive (Tg473K). As the **solder balls** are reflowed prior to die attach, current assembly **houses** will never need the ball mounter to produce the TBGA.
Subfile: B

19/3,AB/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC

6004726 INSPEC Abstract Number: B9810-0170J-015
Title: Thermal performance of tape based **ball grid** array over molded **packages**
Author(s): Edwards, D.; Hundt, P.
Author Affiliation: Texas Instrum. Inc., Dallas, TX, USA
Conference Title: Fourteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (Cat. No.98CH36195) p.169-75
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xvii+255 pp.
ISBN: 0 7803 4486 3 Material Identity Number: XX98-00768
U.S. Copyright Clearance Center Code: 0 7803 4486 3/98/$10.00
Conference Title: Fourteenth Annual IEEE Semiconductor Thermal Measurement and Management Symposium Proceedings 1998
Conference Sponsor: IEEE Components, Packaging, & Manuf. Technol. Soc
Conference Date: 10-12 March 1998 Conference Location: San Diego, CA, USA
Language: English
Abstract: A near chip scale **package** based on area array technology with a tape interposer is thermally evaluated using both computer models and measurement techniques. The **package** is described and compared to the thermal performance of QFPs with comparable physical dimensions. The thermal performance of the **package** has been found to be highly dependent upon the arrangement of the **solder balls** on the interposer and on the die size. The impact of thermal **solder balls** and underfill is investigated, the contribution of a **heat spreader** is described, and **thermal** variation with material composition is studied.
Subfile: B

19/3,AB/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

5953271 INSPEC Abstract Number: B9808-0170J-042
Title: Development of a C4-**BGA** assembly process-innovations in C4 flux and underfill materials
Author(s): Pendse, R.D.; Courtis, M.; Serrano, B.
Author Affiliation: Hewlett-Packard Co., Palo Alto, CA, USA

Conference Title: Proceedings. 1997 International Symposium on Microelectronics (SPIE vol.3235) p.455-61
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 1997 Country of Publication: USA xvii+707 pp.
ISBN: 0 930815 50 5 Material Identity Number: XX98-00801
Conference Title: Proceedings 1997 International Symposium on Microelectronics
Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 14-16 Oct. 1997 Conference Location: Philadelphia, PA, USA
Language: English
Abstract: A controlled collapse chip connection-**ball grid** array (C4-**BGA**) assembly process has been developed for internal manufacturing of high pin count ASIC devices used in HP computers. The process uses high-Pb solder bumps and entails the major unit processes of chip fluxing and placement, reflow, underfilling, **thermal spreader** attachment and **solder ball** attachment. The focus of the present paper is some key innovations made in the area of C4 flux and underfill chemistry that helped reduce process cost. A unique rosin-free flux formulation was developed to implement C4 joining in a nitrogen environment (as opposed to hydrogen environment), despite the high C4 reflow temperatures involved (~350 degrees C peak). This obviated the expensive facilitization of a hydrogen environment which is typically required in conventional C4 reflow ovens. Furthermore, the formulation was optimized to achieve ultra-low flux residue levels. The interaction between the underfill material and trace levels of flux residue was studied to help develop an underfill epoxy that provides good adhesion to the chip surface without performing flux cleaning. This underfill material in conjunction with the low residue flux made it possible to eliminate the C4 cleaning step, thus obviating the use and handling of solvents and cleaning equipment. We present results of extensive testing performed using a C4 test chip with 1,200 bumps assembled to a 11-layer single chip **package** . We also report on results of FTIR and CSAM studies of the materials and the **package** failure modes respectively.
Subfile: B

19/3,AB/15 (Item 15 from file: 2)
DIALOG(R)File 2:INSPEC

5678314 INSPEC Abstract Number: B9710-0170J-031
Title: Reliability results for a wire bondable tape **ball grid** array **package**
Author(s): Schueller, R.D.
Author Affiliation: 3M Electron. Prod. Div., Austin, TX, USA
Conference Title: SMTA National Symposium `Emerging Packaging Technologies' Proceedings of The Technical Program p.71-85
Publisher: Surface Mount Techol. Assoc, Edina, MN, USA
Publication Date: 1996 Country of Publication: USA 138 pp.
Material Identity Number: XX96-03693
Conference Title: Proceedings of Technology in the Park Symposium
Conference Date: 18-21 Nov. 1996 Conference Location: Research Triangle Park, NC, USA
Language: English
Abstract: This paper reviews a new wire bondable tape **ball**

grid array **package** which exhibits a cost/performance advantage in the industry. This novel **package** architecture utilizes the fine line capability of flexible circuitry to provide the high performance and reliability required by the increasingly advanced ICs of today and tomorrow. This TBGA is designed to provide excellent heat dissipation through use of a **heat spreader** to which the die is directly adhered. Heat is therefore efficiently dissipated into surrounding air and into the motherboard. With the capability for less than 50 mu m lines and spaces, the wire bond fingers can be moved in very close to the die, thus minimizing wire bond length and allowing for the possibility of die shrinkage. The resulting decrease in inductance enables **packaging** of high speed devices. This product can be provided at a competitive price, partially due to 3M's efficient process for simultaneous chemical etching of holes in the polyimide substrate to define **solder ball pads**. This paper includes an overview of this **package** as well as detailed results of **package** coplanarity and board level reliability testing. Extrapolations are performed to estimate life in actual use conditions. These results show ample reliability for most applications.

Subfile: B

19/3,AB/16 (Item 16 from file: 2)
DIALOG(R)File 2:INSPEC

5665017 INSPEC Abstract Number: B9709-0170J-051

Title: A comprehensive study on 40-mil **PBGA**

Author(s): Chen, R.T.; Yukon Chou; Ho, T.C.; Chiang, P.H.; Chien-Chi Chao ; Wun-Yan Chen

Author Affiliation: ITRI, Taiwan

Conference Title: Proceedings. 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces (Cat. No.97TH8263) p.62-3

Publisher: IEEE, New York, NY, USA

Publication Date: 1997 Country of Publication: USA viii+183 pp.

ISBN: 0 7803 3818 9 Material Identity Number: XX97-00693

Conference Title: Proceedings 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces

Conference Sponsor: Int. Microelectron. & Packaging Soc. (IMAPS); IEEE Components, Packaging, & Manuf. Technol. Soc.; Georgia Inst. Technol., Pakcaging Res. Center (PRC)

Conference Date: 9-12 March 1997 Conference Location: Braselton, GA, USA

Language: English

Abstract: The 40-mil **PBGA** is an effective application for higher I/O density. In regular consideration, the pad size and the **solder sphere** should be smaller due to decreasing the bump pitch from 50 or 60 mils to 40-mil **PBGA**. Until now, we could not find any standard product or paper which refers to **pad** size and **solder sphere** diameter. So we setup this experiment to find out the results and hope it will be useful to build-up the optimal bumping process of 40-mil **PBGA**. In this study, we considered many different factors such as substrate **pad** size and **solder sphere** diameter. In order to find out the best combination of all these factors to achieve the highest manufacturing yield, we applied the thermocouple technology to

measure the **thermal distribution** of the entire substrate in reflow furnace. After bumping the **solder ball** onto the substrate, we use ball shear test to analyze the force difference between the balls caused by different temperature profile. The shear height and shear speed variables of the ball shear testing are also investigated in this study. The x-section technology was applied in this experiment for examining the bump shape after finishing the bumping process. In this study, we also utilize the noncontact laser technology to examine the bump height after solder bumping process. In order to understand data about SMT application of 40-mil **PBGA**, the solder joint height with different **solder ball** diameter and the reliability test data were both included in this experiment. Of course, we design a test board with daisy chain and utilize the x-section technology to achieve the jobs.

Subfile: B

19/3,AB/17 (Item 17 from file: 2)
DIALOG(R)File 2:INSPEC

5362657 INSPEC Abstract Number: B9610-0170J-038

Title: An enhanced performance low cost **BGA package**

Author(s): Marrs, R.; Molnar, R.; Lynch, B.; Mescher, P.; Olachea, G.
Author Affiliation: Amkor Electron. Inc., Chandler, AZ, USA

Conference Title: SMI Surface Mount International. Advanced Electronics Manufactuting Technologies. Proceedings of the Technical Program p. 214-25
Publisher: SMTA, Edina, MN, USA
Publication Date: 1995 Country of Publication: USA 1082 pp.
Material Identity Number: XX96-01150
Conference Title: Proceedings of Surface Mount International Conference
Conference Date: 29-31 Aug. 1995 Conference Location: San Jose, CA, USA
Language: English

Abstract: This paper reviews a new class of low-cost, thermally and electrically superior, low profile **ball grid** array **packages** called superBGAs (SBGAs), suitable for both low and high I/O applications. SBGAs are tooled in standard JEDEC outlines ranging from 20-680 balls in 7-50 mm body sizes. The SBGA thermal performance is achieved by incorporation of a **heatsink covering** the **package** top surface and a novel method for efficient heat transfer to all of the **solder balls** . ICs are directly attached to the heatsink in a die-down configuration, resulting in maximum **heat spreading** . The enhanced SBGA electrical performance is achieved by design features such as low-inductance conductor paths, microstrip signal lines, efficient power and ground planes, short conductor paths, close proximity power and ground buses to which wire bonds are directly connected, and routing of all signal lines without use of vias or through-holes. Also, SBGAs have very good EMI shielding. The topside of the **package** is 100% shielded, and the grid-like **solder ball** structure provides effective side shielding. The SBGA's design and materials selection has resulted in significantly improved reliability. Advancements have enabled major upgrades in moisture and delamination resistance, **solder ball** fatigue resistance and reduction in both chip and bondwire stress. The **package** consistently demonstrates JEDEC Level 2 (85 degrees C/60%RH/168 hr) preconditioning performance

(sufficient for 1 year factory floor life without baking). This paper includes an overview of the **package** structure, materials, manufacturing process, thermal performance, electrical characteristics and reliability.
Subfile: B

19/3,AB/18 (Item 18 from file: 2)
DIALOG(R)File 2:INSPEC

5176676 INSPEC Abstract Number: B9603-0170J-065
Title: Effect of material properties on the fatigue life of dual **solder** (DS) ceramic **ball grid** array (CBGA) solder joints
Author(s): Puttlitz, K.J.; Caulfield, T.; Cole, M.
Author Affiliation: East Fishkill Facility, IBM Microelectron., Hopewell Junction, NY, USA
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference (Cat. No.95CH3582-0) p.1005-10
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 1293 pp.
ISBN: 0 7803 2736 5 Material Identity Number: XX95-01395
U.S. Copyright Clearance Center Code: 0569-5503/95/0000-1005$3.00
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference
Conference Date: 21-24 May 1995 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: The interconnection structure of industry-standard **ball grid** array (**BGA**) electronic **packages**, both plastic and ceramic, consists of a single alloy, typically eutectic Pb-Sn solder. However, IBM ceramic **BGA packages** utilize a unique dual-solder (DS) interconnection system, which consists of a low-melting alloy (eutectic Pb-Sn) to attach a higher melting alloy ball to the ceramic substrate at one end and card on the opposite end of the joint. Unlike industry-standard **BGA** joints which collapse upon reflow, DS joints do not since their high MP ball does not become molten during processing, providing a reproducible standoff and significant fatigue life advantage. Finite element modeling indicates that the highest stress occurs within the low-MP fillet area, verified by crack patterns generated during accelerated thermal fatigue testing. The purpose of this study was to determine which combination of material properties provide an optimum joint fatigue life. The intent is to more uniformly **distribute thermally** induced strains within the solder connection by transferring some of the stress-relief from within the fillet areas to the ball. Accordingly, several ball and fillet materials were investigated in various combinations ranging in yield, strength and creep resistance properties. Both thermal fatigue data and supporting metallography are presented for the various solder joint combinations investigated.
Subfile: B

19/3,AB/19 (Item 19 from file: 2)
DIALOG(R)File 2:INSPEC

5161562 INSPEC Abstract Number: B9602-0170J-028
Title: A low-cost metal **ball grid** array for flip chip die
Author(s): Wilson, J.W.; Moore, S.P.; Laine, E.H.
Author Affiliation: IBM Corp., Endicott, NY, USA
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference (Cat. No.95CH3582-0) p.42-5
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 1293 pp.
ISBN: 0 7803 2736 5 Material Identity Number: XX95-01395
U.S. Copyright Clearance Center Code: 0569-5503/95/0000-0042$3.00
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference
Conference Date: 21-24 May 1995 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: A low cost **ball grid** array **package** has been developed for use with flip chip die. The structural "back bone" of this chip carrier is a metal plate which serves as a built-in **heat spreader** and a floating ground plane as well as the principal structural member of the **package**. Thin film circuitry is employed to make the necessary connections between the die and the **solder balls** . The fine line circuitization enables escape of many I/O from the flip chip die and thus a high I/O **package** with only a single layer of circuitry. The circuit lines are separated from the metal plate by means of a thin polymer dielectric layer. The die is attached to the carrier with a conventional high temperature C4 attach process. The **ball grid** array is on a 1.27 mm pitch. The metal plate that serves as the structural member of this **package** provides a number of benefits. The coefficient of thermal expansion (CTE) of the metal plate is very close to the CTE of the circuit card. The size of the **package** is not limited, therefore, in order to prevent fatigue and fracture of **solder balls** . The metal plate is separated from the circuitry by only a thin layer of dielectric material. The plate thus serves as a very effective floating ground plane and thereby provides improved electrical performance. The plate also serves as an effective **heat spreader** , again because of the thin dielectric layer separating the metal plate from the circuitry, the die and the **solder balls**. If added thermal performance is desired, a heat sink is easily attached to the backside of the metal plate. The thin film circuitry employed in this **package** also provides a number of benefits. The die and the **solder balls** are connected by a single layer of circuitry. Since electrical vias are not required, low cost processing is possible. Circuitization of the thin film metal can produce extremely fine lines and spaces; more than 700 I/O can be handled in a single layer.
Subfile: B

19/3,AB/20 (Item 20 from file: 2)
DIALOG(R)File 2:INSPEC

4776050 INSPEC Abstract Number: B9411-0170J-024
Title: Capturing design advantages of **BGAs**
Journal: Surface Mount Technology vol.8, no.3 p.36-7, 43
Publication Date: March 1994 Country of Publication: USA

ISSN: 0893-3588
U.S. Copyright Clearance Center Code: 0893-3588/94/$1.00+50
Language: English
Abstract: The construction of the over-molded pad array carrier (OMPAC) begins with a single-layer BT resin epoxy PCB. The die is attached via a gold-plated die attach and a silver-filled epoxy. Conventional plastic transfer molding **encapsulated** the **package** and interconnection between die and epoxy PCB is through thermosonic gold wire bonding. From there copper traces are routed to an array of metal pads on the bottom side of the board to which solder bumps (62 Sn, 36 Pb, 2 Ag) are partially reflowed, providing the **package** with 'leads.' For increased heat dissipation, OMPACs include thermal vias (copper plated-through holes) directly beneath the die. Copper foil serves to **distribute** the **heat** to specific **solder balls**, which are connected to the system PCB (product) ground plane(s).
Subfile: B

19/3,AB/21 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06116927
E.I. No: EIP02357063295
Title: Experimental study on CBGA assembly in various environmental temperatures using moire interferometry
Author: Wang, W.N.; Yang, Y.P.; Wen, X.M.; Jiang, X.L.; Dai, F.L.
Corporate Source: Dept. of Physics Capital Normal Univ., 100037, Beijing, China
Conference Title: 3th Conference on Experimental Mechanics
Conference Location: Beijing, China Conference Date: 20011015-20011017
E.I. Conference No.: 59425
Source: Proceedings of SPIE - The International Society for Optical Engineering v 4537 2001. p 414-417
Publication Year: 2001
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: Solder joints between a ceramic **ball grid** array (CBGA) and a printed circuit (PCB) generally suffer important thermal strains and stresses during the operation of devices as well as under temperature variations. Mainly, these tend to increase the thermal stress concentration in solder joints. In this study, moire interferometry is used to measure the power-induced thermal displacement in the CBGA assembly. The experimental study is performed under various environmental temperatures using different power levels. Two types of **thermal** strain **distributions** are found in the assembly, depending on the thermal loadings. The stress concentrations are located in the CBGA assembly. Then, based on the relative displacement between the CBGA and the PCB, the shear stress on the **solder ball** is determined. Moreover, the effects of different thermal loadings on the CBGA as well as their impact on the reliability of CBGA **solder balls** are discussed in details. 3 Refs.

19/3,AB/22 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05977433
E.I. No: EIP01556801126
Title: Effects of microstructural evolution and intermetallic layer growth on shear strength of **ball-grid** -array Sn-Cu solder joints
Author: Shin, C.K.; Baik, Y.-J.; Huh, J.Y.
Corporate Source: Korea University Div. of Materials Science and Eng., Seoul 136-701, South Korea
Source: Journal of Electronic Materials v 30 n 10 October 2001. p 1323-1331
Publication Year: 2001
CODEN: JECMA5 ISSN: 0361-5235
Language: English
Abstract: The shear strength of **ball-grid**-array (**BGA**) solder joints on Cu bond pads was studied for Sn-Cu solder **containing** 0, 1.5, and 2.5 wt.% Cu, focusing on the effect of the microstructural changes of the bulk solder and the growth of intermetallic (IMC) layers during soldering at 270 degree C and aging at 150 degree C. The Cu additions in Sn solder enhanced both the IMC layer growth and the solder/IMC interface roughness during soldering but had insignificant effects during aging. Rapid Cu dissolution from the **pad** during reflow **soldering** resulted in a fine dispersion of Cu//6Sn//5 particles throughout the bulk solder in as-soldered joints even for the **case** of pure Sn solder, giving rise to a precipitation hardening of the bulk solder. The increased strength of the bulk solder caused the fracture mode of as-soldered joints to shift from the bulk solder to the solder/IMC layer as the IMC layer grew over a critical thickness about 1.2 mum for all solders. The bulk solder strength decreased rapidly as the fine Cu//6Sn//5 precipitates coarsened during aging. As a consequence, regardless of the IMC layer thickness and the Cu content of the solders, the shear strength of **BGA** solder joints degraded significantly after 1 day of aging at 150 degree C and the shear fracture of aged joints occurred in the bulk solder. This suggests that small additions of Cu in Sn-based solders have an insignificant effect on the shear strength of **BGA** solder joints, especially during system use at high temperatures. 25 Refs.

19/3,AB/23 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05823248
E.I. No: EIP01226522191
Title: Thermal characterization of tape **BGA package** by modeling
Author: Jiang-Bo, H.
Corporate Source: Semiconductor Product Group Agilent Tech. Singapore Priv. Ltd., Singapore 618494, Singapore
Conference Title: Microelectronic Yield, Reliability, and Advanced Packaging
Conference Location: Singapure, Singapore Conference Date: 20001128-20001130
E.I. Conference No.: 58048
Source: Proceedings of SPIE - The International Society for Optical Engineering v 4229 2000. p 202-208

Publication Year: 2000
CODEN: PSISDG ISSN: 0277-786X
Language: English
Abstract: In microelectronic industry, numerical modeling is an effective way to predict thermal performance of IC **packages** in the initial development stage. Moreover, thermal simulation can provide a greater understanding of the physics of the problem, allowing designs to be optimized quickly and cheaply, thereby shortening **packaging** development cycle time and keeping expensive experimental measurements to a minimum. In this study, 3-D finite element analysis (FEA) thermal models capturing the details of the **solder ball** and internal structure of the tape **BGA** (TBGA) **package** are developed. Accuracy of the developed FEA models is validated by benchmarking with the measurement for 35mmx35mm 352 TBGA **package**. Numerical results of the thermal performance of the TBGA **package** under various die size and **heat-spreader** remaining thickness are presented. The thermal metrics, Theta-JA (theta//j//a), Psi-JT (psi//J//T), and Psi-JB (psiJB), of the **package** are characterized numerically. Relationships between these three thermal metrics (theta//j//a psi//J//T and psi//J//B) are established. These relationships are useful to correlate one thermal parameter of the **package** to another. 8 Refs.

19/3,AB/24 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05581098
E.I. No: EIP00065197490
Title: Thermal characterization of cavity-down TBGA **package** with flotherm simulation
Author: Cho, Eric; Tan, Eric; Lin, Yur-Tsai
Corporate Source: Flotrend Co, Taipei, Taiwan
Conference Title: 16th IEEE Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)
Conference Location: San Jose, CA, USA Conference Date: 19000321-19000323
E.I. Conference No.: 56893
Source: Annual IEEE Semiconductor Thermal Measurement and Management Symposium 2000. p 68-75
Publication Year: 2000
CODEN: ASTSFA ISSN: 1065-2221
Language: English
Abstract: This paper presents the use of the finite volume analysis method in predicting thermal performance of a TBGA (Tape **Ball Grid** Array) **package** in a **package** level and in a board level, respectively. The effect of **heat spreader** thickness is also analyzed and the results show that the larger the thickness, the lower the junction temperature. However, it is also shown that more than 75% of heat dissipation is conducted away through **solder balls** rather than the **heat spreader**. The **thermal** performance of a TBGA **package** mounted on a real graphic card is next analyzed in the board level and the results are compared with two **PBGA packages**. With other heat sources around the **package** on the graphic card, the corresponding junction temperatures increase dramatically. The thermal performance of the TBGA is superior to that of both **PBGAs**. The results also show that a heat sink module attached on the top of the

package can further improve the thermal performance of the TBGA **package**. (Author abstract) 4 Refs.

19/3,AB/25 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05256079
E.I. No: EIP99034604398
Title: Time-history popcorning analysis of plastic **ball grid** array **package** during solder reflow with fracture mechanics method
Author: Lau, John H.; Ouyang, Chien; Chen, Ray
Corporate Source: Express Packaging Systems, Inc, Palo Alto, CA, USA
Conference Title: Proceedings of the 1998 ASME International Mechanical Engineering Congress and Exposition
Conference Location: Anaheim, CA, USA Conference Date: 19981115-19981120
E.I. Conference No.: 49454
Source: American Society of Mechanical Engineers (Paper) 1998. ASME, Fairfield, NJ, USA. p 1-8
Publication Year: 1998
CODEN: ASMSA4 ISSN: 0402-1215
Language: English
Abstract: The popcorning effect of plastic **ball grid** array (**PBGA**) **packages** is analyzed using the fracture mechanics. A two dimensional time history plan-strain finite element method (FEM) is used to calculate the **thermal** stress **distribution** of the **package** (composite structure) during solder reflow. For the simple approach, an initial crack length, which is obtained from an uncracked structure due to the thermal expansion mismatch of the **package** and by comparing the stress distribution and the strength of the material, is assumed. After the initiation of the crack, the J-integral values and stress intensity factors are calculated with the additional moisture-vaporized pressure acting on the crack surface inside the **package**. For the more regular approach, the J-integral values and stress intensity factors such as K//1 K//2 are calculated for various temperatures and crack lengths and are compared with the interface toughness. (Author abstract) 7 Refs.

19/3,AB/26 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04471973
E.I. No: EIP96083285132
Title: Reliability evaluations on a new tape **ball grid** array (TBGA)
Author: Gainey, Trevor; Stover, Mike; Auray, Michel
Corporate Source: LSI Logic Europe plc
Conference Title: Proceedings of the 1996 IEEE 46th Electronic Components & Technology Conference, ECTC
Conference Location: Orlando, FL, USA Conference Date: 19960528-19960531
E.I. Conference No.: 45119
Source: Proceedings - Electronic Components and Technology Conference 1996. p 1217-1221

Publication Year: 1996
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: Results of a co-operative study of a new type of Tape **Ball Grid** Array (TBGA) are reported. Results obtained by a component manufacturer (LSI Logic) in reliability assessment of this new **package** type are reported together with results obtained during board mounting trials and subsequent reliability stress testing at board level by a system assembly **house** (Bull Electronics Europe). The various test techniques used by the component manufacturer during component qualification will be described and discussed in terms of the potential failure mechanisms detected by each of the stress tests. Likewise the various electrical, thermal and mechanical tests applied to the mounted **package** are also discussed in relationship to the end use environment. Results are presented of **package** level tests together with those of **packages** mounted to boards both with and without an external heatsink. The study concludes that with careful **package** design and construction together with good board assembly and heatsink attachment methods applied to the **package,** a highly reliable **package** and board assembly system can be achieved. (Author abstract) 4 Refs.

19/3,AB/27 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03951379
E.I. No: EIP94071340057
Title: Capturing design advantages of **BGAs**
Author: Houchten, Jon
Corporate Source: Motorola's Application Specific Integrated Circuits Div, Chandler, AZ, USA
Source: Surface Mount Technology v 8 n 3 Mar 1994. 3p
Publication Year: 1994
CODEN: SMTEEL ISSN: 0893-3588
Language: English
Abstract: ASICs, memories, microprocessors, and analog products are now becoming available in **ball grid** array **packages.** Motorola's version - the Over-Molded Pad Array Carrier - is an adaptation of the technology that seeks to overcome some **BGA** "caution signals". For increased heat dissipation, OMPACs include thermal vias (copper plated-through holes) directly beneath the die. Copper foil serves to **distribute** the **heat** to specific **solder balls,** which will be connected to the system PCB product ground planes.

19/3,AB/28 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03142318 JICST ACCESSION NUMBER: 97A0413787 FILE SEGMENT: JICST-E
Thin-Profile **Ball Grid** Array **Package** with High Thermal Performance.
YANO KEIICHI (1); ASAI HIRONORI (1); IWASE NOBUO (1)
(1) Toshiba Corp.
Toshiba Rebyu(Toshiba Review), 1997, VOL.52,NO.4, PAGE.55-58, FIG.6, TBL.2

JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Toshiba has developed a **ball grid** array(**BGA**) **package** usable for LSIs having up to 5W dissipation without a cooling fin and under natural convection. The assembled height of the **package** mounted on a printed wiring board has been lowered to less than 2mm, and the thickness of the substrate is 0.6mm. High thermal conductive and electrically insulating aluminum nitride(AlN) was selected for the substrate material, and **solder balls** were arranged underneath the LSI. This configuration increases the acceptable LSI dissipated power as it enhances the effect of **heat radiation** to the printed wiring board. Fine-pitch wiring technology was also developed in order to reduce the number of layers and the thickness of the substrate. This **package** is applicable to multimedia devices that handle a large amount of information. (author abst.)

19/3,AB/29 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

2051869 H.W. WILSON RECORD NUMBER: BAST94001319
Thermal modeling of the infrared reflow process for **Solder Ball** Connect (SBC)
Mahaney, H. V;
IBM Journal of Research and Development v. 37 (Sept. 1993) p. 609-19
DOCUMENT TYPE: Feature Article ISSN: 0018-8646

ABSTRACT: A thermal model of the infrared reflow process has been developed for an FR-4 card populated with an array of **Solder Ball** Connect (SBC) modules. The analysis of the three-dimensional, transient, finite element model accounts for radiative exchange within the infrared oven and for the heat conduction (nonisotropic) within the modules and card. Transient temperature profiles of selected points and three-dimensional temperature distributions at selected times are presented to describe the primary heat-transport mechanisms. Numerical predictions and empirical data indicate that the SBC modules are relatively isothermal throughout the infrared reflow process. Therefore, every **solder ball** within the array exhibits a nearly identical thermal profile. This result is fortunate, since the inner **solder ball** connections cannot be visually inspected. The influence of module spacing and the ability to improve the reflow process by use of a high-emissivity cap coating are demonstrated. Reprinted by permission of the publisher. .

19/3,AB/30 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14087813 PASCAL No.: 99-0280975
Effect of **heat-spreader** sizes on the **thermal** performance of large cavity-down plastic **ball grid** array

packages : NuCSP
LAU J; CHEN T
Express Packaging Systems, Inc., Palo Alto, California, United States
Journal: Microelectronics international, 1999, 16 (2) 24-33
Language: English
The effect of **heat-spreader** sizes on the temperature **distribution, thermal** resistance, and cooling power of a set of cost-effective cavity-down plastic **ball grid** array (**PBGA**) **packages** assembled on an FR-4 epoxy glass printed circuit board (PCB) is presented. The sizes of these **packages** are 35 x 35mm and 40 x 40mm and with four and five rows of **solder balls**.

22/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7161249 INSPEC Abstract Number: B2002-02-2250-006
Title: Low cost and high effective thermal management using **PBGA** MCM **package**
Author(s): Kim, S.G.; Chung, D.E.; Woo, J.H.; Lim, S.W.; Lee, C.K.
Author Affiliation: In-Tech Wave Co., Kyungsangbuk, South Korea
Conference Title: Proceedings 2000 International Symposium on Microelectronics (SPIE Vol.4339) p.518-23
Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA
Publication Date: 2000 Country of Publication: USA xx+886 pp.
ISBN: 0 930815 62 9 Material Identity Number: XX-2001-01666
Conference Title: 2000 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS - Int. Microelectron. & Packaging Soc
Conference Date: 18-20 Sept. 2000 Conference Location: Boston, MA, USA
Language: English
Abstract: The MCM **package** is designed to put together effective **heat spreading** for high power consumption with low costs through functional adaptability and practical integrability. This paper describes the development of Network Interface Module MCM (NIM MCM) for PCS on the basis of MCM-L. NIM MCM consists **PBGA package** with 323 I/O and a ball pitch of 1.27 mm. The **package contains** four ASICs with dimensions 0.43*0.44 inch/sup 2/ each, the 1.62*1.62 inch/sup 2/ **package** , and Al Lid The substrate is a high Tg epoxy build-up structure with 12 **metal** layers, 3/3 mil line width/space, 4/10 mil micro via and represents a highly integrated high power **package**. Especially, NIM MCM is designed for outdoor usage and therefore, requires effective **heat spreading** at the **high** ambient **temperature** with power consumption of 5.3 watt. So. the used MCM-L substrate **contains metal** inside for signal layer, and a separate **metal** core is considered for heat simulation and optimization, and is designed to transfer the heat to the thermal via and then to the ceramic lid. The reliability of the MCM is validated through a series of TC, hermeticity, THB, thermal shock and moisture resistance tests. By using the MCM-L the module size is reduced down to the 25% of common dimensions, efficient **heat spreading** at low cost is actually achieved.
Subfile: B

22/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6750597 INSPEC Abstract Number: B2000-12-0170J-078
Title: Design, manufacturing, and testing of a novel plastic **ball grid** array **package**
Author(s): Lau, J.; Chang, C.; Chen, T.; Tsung-Yuan Chen; Tzyy Jang Tseng ; Cheng, D.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Journal of Electronics Manufacturing vol.9, no.4 p.283-91
Publisher: World Scientific,

Publication Date: Dec. 1999 Country of Publication: Singapore
CODEN: JELMEK ISSN: 0960-3131
SICI: 0960-3131(199912)9:4L.283:DMTN;1-P
Material Identity Number: F164-2000-004
Language: English
Abstract: The design, manufacturing, analysis, and measurement of a thermally and electrically enhanced cavity-down plastic **ball grid** array (**PBGA**) **package** are presented in this study. Due to the split via connection (SVC) design, the **package** consists of a very-thin single core of organic material and two-**metal** layers of copper and is manufactured with a conventional printed circuit board (PCB) process at very low cost. Furthermore, the **heat spreader** is made with a bottom surface with saw-teeth to contact the ground planes disposed on the substrate backside. Improvements in electrical and thermal performance are achieved. Parasitic parameters of the **package** are extracted from time domain reflectometer (TDR) measurements. The thermal performances of the **packages** are studied by both 3D finite element analysis and wind-tunnel measurements. The results are compared with other well-known **packages**.
Subfile: B

22/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6635331 INSPEC Abstract Number: B2000-08-0170J-056
Title: Design, analysis, and measurement of a novel plastic **ball grid** array **package**
Author(s): Lau, J.; Chih-Chiang Chen; Chang, C.; Chen, T.; Huabo Chen; Tsung-Yuan Chen; Tzyy Jang Tseng; Cheng, D.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Conference Title: SMTA International. Proceedings of Technical Program. Conference Proceedings p.202-10
Publisher: Surface Mount Tech. Assoc, Edina, MN, USA
Publication Date: 1999 Country of Publication: USA 659 pp.
Material Identity Number: XX-1999-03096
Conference Title: Proceedings of SMTA International
Conference Date: 12-16 Sept. 1999 Conference Location: San Jose, CA, USA
Language: English
Abstract: The design, analysis, and measurement of a thermally and electrically enhanced cavity-down plastic **ball grid** array (**PBGA**) **package** are presented in this study. Due to the split via connection (SVC) design, the **package** consists of a very thin single core of organic material and two **metal** layers of copper and is manufactured with a conventional printed circuit board (PCB) process at very low cost. Furthermore, the **heat spreader** is made with a saw-tooth bottom surface to contact the ground planes on the substrate backside. Improvements in electrical and thermal performance are achieved. **Package** parasitic parameters are extracted from time domain reflectometer (TDR) measurements. The **package** thermal performance is studied by both 3D finite element analysis and wind-tunnel measurements. The results are compared with other well-known **packages**.
Subfile: B

22/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6307274 INSPEC Abstract Number: B1999-09-0170J-023
Title: EBGA: high frequency electrical characterization and the influence of substrate design parameters on **package** performance
Author(s): Qiu, Y.; Iyer, M.K.; Chong, K.C.; Zhang, T.L.; Rasiah, I.
Author Affiliation: Inst. of Microelectron., Singapore
Conference Title: Proceedings of 2nd Electronics Packaging Technology Conference (Cat. No.98EX235) p.107-11
Editor(s): Tay, A.A.O.; Thiam Beng, L.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1998 Country of Publication: USA 361 pp.
ISBN: 0 7803 5141 X Material Identity Number: XX-1999-00947
U.S. Copyright Clearance Center Code: 0 7803 5141 X/98/$10.00
Conference Title: Proceedings of 2nd Electronics Packaging Technology Conference
Conference Sponsor: IEEE CPMT Soc.; ASME; IMAPS; Gintic Inst. Manuf. Technol.; Inst. Mater. Res. & Eng.; Inst. Microelectron.; Nanyang Technol. Univ.; Nat. Univ. Singapore
Conference Date: 8-10 Dec. 1998 Conference Location: Singapore
Language: English
Abstract: Thermally enhanced **ball grid** array (EBGA) **packages** are studied for their electrical performance and the results are reported in this paper. The electrical parasitics of these EBGA **packages** are extracted in the frequency domain. A performance comparison between EBGA **packages** considering their different design parameters has been conducted and is reported here. The resonance issues related to the **metal heat spreader** are also discussed.
Subfile: B

22/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6294483 INSPEC Abstract Number: B1999-08-0170J-103, C1999-08-7410D-074
Title: Floating **metal** plane on thermal and electrical performance of an enhanced plastic **ball grid** array **package**
Author(s): Kabir, H.; Groover, R.; Tovar, D.; Joroski, J.
Author Affiliation: ChipPAC Inc., Chandler, AZ, USA
Conference Title: Surface Mount International Conference and Exposition. SMI 98. Proceedings p.769-76
Publisher: SMTA, Edina, MN, USA
Publication Date: 1998 Country of Publication: USA 807 pp.
Material Identity Number: XX-1998-02769
Conference Title: Proceedings of Surface Mount International Conference and Exhibition
Conference Date: 23-27 Aug. 1998 Conference Location: San Jose, CA, USA
Language: English
Abstract: Three-dimensional finite element models of a cavity down thin and thermally enhanced **BGA** (T/sup 2/**BGA**) **package** have

been developed using the ANSYS/sup TM/ finite element simulation code. This model has been used for thermal characterization of this **package** under different cooling (air flow) conditions and to investigate the effects of **heat spreader** thickness on **package** junction to ambient thermal resistances for no air flow condition. The influence of the **heat spreader** on electrical parasitics is studied by developing 3D inductance and capacitance models of representative **package** sections using a commercially available software from Pacific Numerix. The effect of a floating **heat spreader** on the frequency-dependent partial inductance of a **package** interconnect is investigated. The effect of the **heat spreader** on simultaneous switching noise is also discussed.
Subfile: B C

22/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5981072 INSPEC Abstract Number: B9809-0170J-011
Title: An EPBGA alternative
Author(s): Karnezos, M.
Author Affiliation: Signetics KP, San Jose, CA, USA
Journal: Advanced Packaging vol.7, no.5 p.90, 92, 94, 96
Publisher: IHS Publishing Group,
Publication Date: June 1998 Country of Publication: USA
ISSN: 1065-0555
SICI: 1065-0555(199806)7:5L.90:EA;1-U
Material Identity Number: F109-98003
Language: English
Abstract: Cavity-up plastic **ball grid** array **packages** (**PBGA**) with a two-layer PCB substrate have the lowest cost but have limited thermal and electrical performance. Versions with a four-layer substrate, called enhanced **PBGAs** (EPBGA), provide higher power dissipation (up to 4 W) with additional power and ground planes for shorter routes and lower noise and electrical parasitics, but their cost is significantly greater. Also, although routing more than five rows of solder bumps at 1.27 mm pitch requires more layers, only marginally improved thermal performance is achieved. Cavity-down **BGAs** generally provide higher performance (and higher cost) compared to their cavity-up counterparts. They consist of an integral **spreader** for better **heat** dissipation and a multilayer substrate with power and ground planes for low noise/parasitics. The die is mounted in the cavity and wire bonded to the substrate, followed by **encapsulation**. The die and solder bumps are arrayed on the bottom of the **package** and compete for the same surface area. For this reason, cavity-down **BGAs** (particularly smaller-body versions) cannot accommodate the larger die sizes possible in cavity-up **PBGAs** . There are numerous other differences among the various cavity-down **BGAs** that also can affect performance and cost and depend on the substrate and **heat spreader** choice. In this article, the design, construction, performance and advantages of a tape **ball grid** array (TBGA) with a single **metal** layer flex substrate and a ground plane with laminated **heat spreader** are proposed as an alternative.
Subfile: B

22/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5961230 INSPEC Abstract Number: B9808-0170J-080
Title: Thermal performance of a low-cost thermal enhanced plastic **ball grid** array **package**-NuBGA
Author(s): Lau, J.H.; Chen, K.L.; Wu, F.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Microelectronics International vol.15, no.2 p.25-33
Publisher: MCB University Press,
Publication Date: May 1998 Country of Publication: UK
CODEN: MIINF2 ISSN: 1356-5362
SICI: 1356-5362(199805)15:2L.25:TPCT;1-8
Material Identity Number: D084-98002
Language: English
Abstract: NuBGA is a low-cost, single-core, double-**metal** layer, cavity down plastic **ball grid** array **package**. With special design concepts, NuBGA provides electrical and thermal enhancements for electronic **packaging** applications. The concepts of these innovative designs are briefly described. The thermal resistance of the junction to air is investigated first by finite element simulations, and the results are then compared to experimental measurements. Also, thermal measurements are carried out both with and without heat sink attachment. Geometric dependence of thermal resistance on structural parameters such as the thickness of the copper **heat spreader** and organic substrate, the power and ground planes in the printed circuit board (PCB), and the PCB size are also discussed.
Subfile: B

22/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

5851114 INSPEC Abstract Number: B9804-0170J-050
Title: Electrical design of a cost-effective thermal enhanced plastic **ball grid** array **package**-NuBGA
Author(s): Lau, J.H.; Tai-Yu Chou
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: IEEE Transactions on Components, Packaging and Manufacturing Technology, Part B: Advanced Packaging vol.21, no.1 p.35-42
Publisher: IEEE,
Publication Date: Feb. 1998 Country of Publication: USA
CODEN: IMTBE4 ISSN: 1070-9894
SICI: 1070-9894(199802)21:1L.35:EDCE;1-Y
Material Identity Number: B481-98001
U.S. Copyright Clearance Center Code: 1070-9894/98/$10.00
Language: English
Abstract: An electrically and thermally optimized plastic **ball grid** array (**PBGA**) **package**, called new and useful **ball grid** array (NuBGA) is presented. NuBGA is a cavity down **package** with a **metal heat spreader covering** the entire back-side of the chip. The **heat spreader** is

laminated with a single-core double-sided organic substrate. Super electrical performance is achieved by using the split-wrap-around (SWA) or split-via-connection (SVC) design concepts. All traces on the core substrate are designed into mu -stripline and co-planar stripline structures. In this paper, the focus is on (1) the unique design concepts; (2) the electrical measurement; (3) the electrical analysis; (4) the electrical performance comparison with other standard **packages**.
Subfile: B

22/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

5709572 INSPEC Abstract Number: B9711-0170J-064
Title: Thermal evaluation of a cost-effective plastic **ball grid** array **package**-NuBGA
Author(s): Wu, F.; Lau, J.; Chen, K.-L.
Author Affiliation: Express Package Syst. Inc., Palo Alto, CA, USA
Conference Title: 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048) p.309-18
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 1294 pp.
ISBN: 0 7803 3857 X Material Identity Number: XX97-01595
U.S. Copyright Clearance Center Code: 0 7803 3857 X/97/$4.00
Conference Title: 1997 Proceedings 47th Electronic Components and Technology Conference
Conference Sponsor: Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Conference Date: 18-21 May 1997 Conference Location: San Jose, CA, USA
Language: English
Abstract: NuBGA is a low cost, single core, two-**metal** layer, cavity down plastic **ball grid** array **package**. With special design concepts, NuBGA provides electrical and thermal enhancements for electronic **packaging** applications. In this paper, the concepts of these innovative designs are briefly described. Thermal resistance of junction to air is investigated first by finite element simulations, and the results are then compared to experimental measurements. Thermal measurements are carried out for both with and without heat sink attachment. Geometric dependence of thermal resistance on structural parameters such as thickness of the copper **heat spreader** and organic substrate, power and ground planes in print circuit board, and the size of PCB are also discussed.
Subfile: B

22/3,AB/10 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05024764
E.I. No: EIP98054215819
Title: Proceedings of the 1998 IEEE 14th Annual Semiconductor Thermal Measurement and Management Symposium
Author: Anon (Ed.)

Conference Title: Proceedings of the 1998 IEEE 14th Annual Semiconductor Thermal Measurement and Management Symposium
Conference Location: San Diego, CA, USA Conference Date: 19980310-19980312
E.I. Conference No.: 48417
Source: Annual IEEE Semiconductor Thermal Measurement and Management Symposium 1998. IEEE, Piscataway, NJ, USA,98CH36195. 255p
Publication Year: 1998
CODEN: ASTSFA ISSN: 1065-2221
Language: English
Abstract: The proceedings **contains** 23 papers from the 1998 IEEE 14th Annual Semiconductor Thermal Measurement and Management Symposium. Topics discussed include: microwave integrated circuits; heat sinks; thermal benchmark chips; multiple output devices; plastic **ball grid** arrays (**PBGA**); **heat spreaders thermal** interface materials; high-power electronics modules; thermal management; electromigration failure; additive multilayer circuitry; chip level thermal effects; and thermal characterization.

22/3,AB/11 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04416288
E.I. No: EIP96063203603
Title: Electrical characterization of a tape **ball grid** array **package**
Author: Harvey, Paul; Kinningham, Alan; Schmolze, Chris
Corporate Source: 3M Electronic Products Div, Austin, TX, USA
Conference Title: Proceedings of the 1995 International Electronics Packaging Conference, IEPS
Conference Location: San Diego, CA, USA Conference Date: 19950924-19950927
E.I. Conference No.: 44728
Source: Proceedings of the International Electronics Packaging Conference 1995. IEPS, Wheaton, IL, USA. p 775-786
Publication Year: 1995
CODEN: 002366
Language: English
Abstract: TBGA product based on 1ML and 2ML taped is measured and analyzed for electrical performance. Models of the parasitic electrical parameters are developed with good agreement to the measured data. Analysis of the results indicates that many key electrical parameters are significantly different in the 1ML and 2ML TBTA versions. Frequency domain analysis does not indicate any significant resonance below 1GHz and confirms validity of the equivalent circuit model to switching speeds of approximately 300 ps. These results indicate that TBGA **packaging** technology compare favorably with plastic **BGA** and other competitive **packaging** technologies. 11 Refs.

22/3,AB/12 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04416270

E.I. No: EIP96063203585
Title: **Ball grid** array type **package** by using of new **encapsulation** method
Author: Kawahara, T.; Kasai, J.; Osawa, M.; Ishiguro, H.; Kato, Y.; Sakurai, Y.; Nakaseko, S.; Hozumi, T.
Corporate Source: Fujitsu Ltd, Kawasaki, Jpn
Conference Title: Proceedings of the 1995 International Electronics Packaging Conference, IEPS
Conference Location: San Diego, CA, USA Conference Date: 19950924-19950927
E.I. Conference No.: 44728
Source: Proceedings of the International Electronics Packaging Conference 1995. IEPS, Wheaton, IL, USA. p 577-587
Publication Year: 1995
CODEN: 002366
Language: English
Abstract: New **ball grid** array (**BGA**) type **package** with the characteristics in the structure of interposer and the **encapsulation** method and the composition of **encapsulant** was developed. This paper proposes new structure of **BGA package** called transfer molding method. The maximum characteristic of the proposed **package** structure is that neither so-called runner, gate nor cavity exist completely. Furthermore, high cost effectivity is achieved, because the mold structure becomes extremely simple. As a result, special **encapsulant** with extremely strong adhesive strength is applied and high reliability is able to be obtained. 2 Refs.

22/3,AB/13 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03545011 JICST ACCESSION NUMBER: 98A0467041 FILE SEGMENT: JICST-E
Semiconductor Devices. Semiconductor Devices for Computers Systems. ASICs.
High Pin Count and High-frequency Operation LSI **Package** for ASIC.
YAJIMA KEI (1); NAKAO HIROSHI (1); KAJIHARA MAMORU (1); BABA MIKIO (1); FURUYA KENJI (1); DOBASHI MASAHIRO (2)
(1) NEC Corp.; (2) NECEnjiniaringu
NEC Giho(NEC Technical Journal), 1998, VOL.51,NO.3, PAGE.103-105, FIG.3, TBL.2
JOURNAL NUMBER: G0475BAB ISSN NO: 0285-4139
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.5
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Introduction article
MEDIA TYPE: Printed Publication
ABSTRACT: NEC has developed the Flip Chip **Ball Grid** Array(FCBGA) **package** as high pin count and high-frequency operation ASIC with 0.25 micron and the further more generation. This **package** has an organic substrate as an interposer, high melting point solder bump with eutectic solder as the connection between die and substrate, and underfill resin and **heat spreader** which are directly placed on the backside of die for power dissipation. This **package** also achieves long-term reliability. (author abst.)

25/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6635332 INSPEC Abstract Number: B2000-08-0170J-057
Title: High thermal performance tape **BGA** for media processor
Author(s): Ohtaka, T.; Yoshioka, O.; Sugimoto, H.; Ohmori, T.; Suzuki, S.
Author Affiliation: Syst. Mater. Lab., Hitachi Cable Ltd., Ibaraki, Japan
Conference Title: SMTA International. Proceedings of Technical Program. Conference Proceedings p.211-17
Publisher: Surface Mount Tech. Assoc, Edina, MN, USA
Publication Date: 1999 Country of Publication: USA 659 pp.
Material Identity Number: XX-1999-03096
Conference Title: Proceedings of SMTA International
Conference Date: 12-16 Sept. 1999 Conference Location: San Jose, CA, USA
Language: English
Abstract: Currently, the I/O counts, frequency and power for media processors such as graphic accelerators and modem controllers are rapidly increasing. This trend changes the **packaging** structure of media processors. The current main substrate for media processor is the **PBGA**; however, the **PBGA** has limited thermal performance. The tape **BGA** (TBGA) has been developed for high thermal performance with **BGA** construction. The TBGA consists of TAB tape and a **heat spreader**, and as the **heat spreader** is made from pure **copper**, the thermal performance is about twice that of the **PBGA**. As TAB provides a very high density circuit pattern and is thin, the TBGA **package** size is smaller and thinner than that of **PBGAs**. These features are suited to media processor applications, and thus the TBGA is becoming the standard substrate for media processors.
Subfile: B

25/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6392388 INSPEC Abstract Number: B1999-12-0170J-062
Title: The effects of **heat spreader** surface treatment and adhesives on the **package** reliability of 304-pin high power **BGA** (L3BGA)
Author(s): Park, I.S.; Kang, I.S.; Kim, J.S.; Heo, S.J.; Song, C.J.
Author Affiliation: Package R&D Team, LG Semicon Co. Ltd., Cheong-Ju, South Korea
Journal: Proceedings of the SPIE - The International Society for Optical Engineering Conference Title: Proc. SPIE - Int. Soc. Opt. Eng. (USA) vol.3582 p.577-82
Publisher: SPIE-Int. Soc. Opt. Eng,
Publication Date: 1999 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
SICI: 0277-786X(1999)3582L.577:EHSS;1-Z
Material Identity Number: C574-1999-173
Conference Title: 1998 International Symposium on Microelectronics
Conference Sponsor: SPIE; IMAPS
Conference Date: 1-4 Nov. 1998 Conference Location: San Diego, CA, USA

Language: English
Abstract: With the increasing device speed and power, excellent heat dissipation is required in electronic **packages**. One solution is the high power **BGA**, which consists of a **heat spreader** and a printed wiring substrate. However, adhesion reliability becomes an issue, as occasional delamination of the **Cu heat spreader** from the printed wiring substrate can create a reliability problem in high power **BGA** devices. Adhesive type and properties strongly affect the adhesion reliability. Oxide treatment increases the surface roughness and increases the adhesion strength and adhesion reliability. Although the adhesion strength of two types of **heat spreaders**, bare and oxide-treated **heat spreaders**, are similar, the pressure cooker test (PCT) shows much higher adhesion reliability in the oxide-treated **heat spreader** for some adhesives, but not for others. According to SEM and XPS analysis, delamination occurs inside the adhesive or the interface or in a mixture of the two. Adhesion strength and moisture absorption are the major factors affecting the delamination of the L3BGA **package**. To reduce delamination between the **heat spreader** and printed wiring substrate, low moisture absorption and high adhesion and adhesion reliability are necessary.
Subfile: B

25/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6307519 INSPEC Abstract Number: B1999-09-0170J-055
Title: Thermal and mechanical evaluations of a cost-effective plastic **ball grid** array **package**
Author(s): Kuan-Luen Chen; Lau, J.H.; Wu, F.H.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Conference Title: Proceedings of the Technical Program. NEPCON West '97. Conference Part vol.2 p.1042-54 vol.2
Publisher: Reed Exhibition, Norwalk, CT, USA
Publication Date: 1997 Country of Publication: USA 3 vol. 1754 pp.
Material Identity Number: XX-1999-01550
Conference Title: Proceedings of NEPCON West '97
Conference Date: 23-27 Feb. 1997 Conference Location: Anaheim, CA, USA
Language: English
Abstract: The temperature **distribution** and **thermal** resistance of a face-down **PBGA** (Plastic **Ball Grid** Array) **package** assembled on a FR-4 epoxy glass PCB (Printed Circuit Board) are presented. By varying the thickness of the **copper heat spreader** and organic substrate, an optimum **PBGA package** is designed. The effect of power and ground planes in the PCB and the size of PCB on the thermal performance of the **PBGA** is also given. Furthermore, the warpage (deflection) of the **package** under thermal loading is predicted.
Subfile: B

25/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6282607 INSPEC Abstract Number: B1999-08-0170J-016, C1999-08-7410D-024
Title: Parametric study of thermal performance of a plastic **ball grid** array, single **package** technology for automotive applications
Author(s): Ramakrishna, K.; Trent, J.R.
Author Affiliation: Adv. Interconnect Syst. Labs., Motorola Inc., Austin, TX, USA
Conference Title: CAE/CAD and Thermal Management Issues in Electronic Systems. 1997 ASME International Mechanical Engineering Congress and Exposition p.13-21
Editor(s): Agonafer, D.; Amon, C.H.; Belady, C.; Kowalski, G.; Orgega, A.
Publisher: ASME, New York, NY, USA
Publication Date: 1997 Country of Publication: USA v+109 pp.
ISBN: 0 7918 1852 7 Material Identity Number: XX-1999-00994
Conference Title: CAE/CAD and Thermal Management Issues in Electronic Systems. ASME International Mechanical Engineering Congress and Exposition
Conference Sponsor: ASME
Conference Date: 16-21 Nov. 1997 Conference Location: Dallas, TX, USA
Language: English
Abstract: Thermal performance of a three chip **BGA** single **package** technology (SPT) has been evaluated under horizontal natural convection conditions for under-the-hood automotive applications by solving a conjugate heat transfer problem to determine the maximum junction temperatures as a function of ambient temperature and material parameters. The resulting conjugate heat transfer problem is solved using computational fluid dynamics (CFD) methods. The SPT provides **packaging** of all dice on a single wire bonded plastic **ball grid** array (**PBGA**) four layer BT substrate. All dice are **encapsulated** in a single mold compound block. The SPT is attached to a 1.52 mm thick, four-layer (with two solid internal **copper** planes) FR4 PWB. The multi-dimensional heat transfer effects in the vias and the C5 solder joints are taken into account through a separate sub-model approach and the effective conductivity is used in the CFD model. The actual stack-ups of the BT substrate and PWB are used in the CFD analysis. Radiative loss from the exposed surfaces of the **package** and the PWB to the ambient is included. Since the objective here is the assessment of stand-alone **package** level thermal performance of the SPT, it is assumed that no other components are dissipating power on the PWB. The transient conjugate problem is also solved for power up of the **package** initially at an ambient temperature of 125 degrees C for a power dissipation of 7 W. CFD simulations of the transient have been carried out for 7 s after the die is powered up.
Subfile: B C

25/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5798985 INSPEC Abstract Number: B9802-0170J-049, C9802-7410D-086
Title: Thermal and mechanical evaluations of a cost-effective plastic **ball grid** array **package**
Author(s): Lau, J.H.; Chen, K.-L.
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA
Journal: Transactions of the ASME. Journal of Electronic Packaging

vol.119, no.3 p.208-12
Publisher: ASME,
Publication Date: Sept. 1997 Country of Publication: USA
CODEN: JEPAE4 ISSN: 1043-7398
SICI: 1043-7398(199709)119:3L.208:TMEC;1-U
Material Identity Number: N602-97004
U.S. Copyright Clearance Center Code: 1043-7398/97/$3.00
Language: English
Abstract: The temperature **distribution** and **thermal** resistance of a facedown **PBGA** (plastic **ball grid** array) **package** assembled on a FR-4 epoxy glass PCB are presented. By varying the thickness of the **copper heat spreader** and organic substrate, an optimum **PBGA package** is designed. The effects of the PCB power and ground planes and the size of PCB on the thermal performance of the **PBGA** are also given. Furthermore, the warpage (deflection) of the **package** under thermal loading is predicted.
Subfile: B C

25/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5495132 INSPEC Abstract Number: B9703-0170J-057
Title: A study of the thermal performance of **BGA packages**
Author(s): Guenin, B.M.; Lall, B.S.; Molnar, R.J.; Marrs, R.C.
Author Affiliation: Adv. Products Oper., Amkor Electron. Inc., Chandler, AZ, USA
Conference Title: Proceedings. 1995 International Flip Chip, Ball Grid Array, TAB and Advanced Packaging Symposium, ITAP '95 p.37-46
Publisher: Semicond. Technol. Center, Neffs, PA, USA
Publication Date: 1995 Country of Publication: USA 299 pp.
Material Identity Number: XX95-00477
Conference Title: Proceedings 1995 International Symposium on Flip Chip, Tab & Ball Grid Array Technology
Conference Date: 14-17 Feb. 1995 Conference Location: San Jose, CA, USA
Language: English
Abstract: A non-linear, lumped-parameter model for the Plastic **BGA** (**PBGA**) **package** has been developed. It incorporates analytical expressions for 2-D **heat spreading** in both the **package** laminate and the external circuit board. The predictions of the model were shown to be in reasonable agreement with experimentally measured values in natural, mixed, and forced convection regimes. The model was used to predict the thermal performance of **PBGA packages** with laminates of varying **copper** content. These results were compared with those produced for a SBGA (SuperBGA(R)) **package** of the same size by a model previously developed for that **package** type. The subsequent analysis was used to evaluate the thermal performance of **PBGA** and SBGA **packages**. It was shown that the concept of a **package heat Spreading** Factor is very useful in understanding the effect of increasing the **copper** content of a **package** on its thermal performance. An increase in the **package** Spreading Factor (SF) reduces Theta /sub JA/ primarily by reducing Theta /sub J-BOARD/ by means of an accompanying increase in the area of the laminate participating in the transfer of heat to the board. An increase in the Spreading Factor has the

secondary effect of reducing Theta /sub BOARD-TO-AIR/ by increasing the thermal footprint of the **package** for heat injection into the board. The thermal performance superiority of the SBGA **package** over a thermally-enhanced, **PBGA** having a 4-layer laminate was demonstrated and rationalized by reference to the much higher Spreading Factor in the SBGA **package**.
Subfile: B

25/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

5161558 INSPEC Abstract Number: B9602-0170J-024
Title: High I/O plastic **ball grid** array **packages**-AT&T Microelectronics experience
Author(s): Cohn, C.; Richman, R.M.; Saxena, L.S.; Shih, M.T.
Author Affiliation: AT&T Bell Labs., Allentown, PA, USA
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference (Cat. No.95CH3582-0) p.10-20
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 1293 pp.
ISBN: 0 7803 2736 5 Material Identity Number: XX95-01395
Conference Title: 1995 Proceedings. 45th Electronic Components and Technology Conference
Conference Date: 21-24 May 1995 Conference Location: Las Vegas, NV, USA
Language: English
Abstract: AT&T Microelectronics **package** requirements for complex high-performance 0.5 mu m ASIC devices are currently in the 225 to 640 I/O range, 60 to 150 MHz, and 2 to 10 watt power dissipation. These requirements can be met with the traditional multilayer Ceramic Pin Grid Array (CPGA) **packages** or the lower Cost Plastic Pin Grid Array (PPGA). However, the ceramic and plastic PGAs are unwieldy and expensive at high I/O counts. Furthermore, through-hole **packages** are undesirable for customers who have switched to complete surface mount assembly lines. The plastic **ball grid** array (**BGA**) is a solution for lower cost, high I/O, high performance, surface mount and small outline **package** requirements. Using our extensive experience with plastic PGAs, we have extended the **BGA** technology to meet higher I/O and performance requirements. During the past two years we designed, developed and fabricated 235-388 I/O, four layer **BGA packages**. A 1995 production ramp up is under way. For improved electrical performance, vias were positioned to minimize trace lengths. Thermal performance was enhanced by the placement of thermal vias under the chip and direct connections to the ground plane. We have pursued two parallel **BGA** manufacturing paths with two different technologies: (a) overmolded **BGAs** through subcontract assembly; (b) Cavity type, liquid epoxy **encapsulated** for in-**house** assembly capability. Both types of **BGA** structures meet AT&T- ME`s device qualification requirements and can be used to ship product. We are currently developing high performance 560 and 640 **BGAs** in a cavity down configuration. The **packages** will have power and ground planes and the chip will be directly attached to a **heat spreading Cu** slug. We are planning to offer the high performance **BGAs** in the 1996 time frame.
Subfile: B

25/3,AB/8 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05994213
E.I. No: EIP01446711620
Title: Advanced thermal interface materials for enhanced flip chip **BGA**
Author: Kohli, P.; Sobczak, M.; Bowin, J.; Matthews, M.
Corporate Source: Ablestik Laboratories, Rancho Dominguez, CA, United States
Conference Title: 51st Electronic Components and Technology Conference
Conference Location: Orlando, FL, United States Conference Date: 20010529-20010601
E.I. Conference No.: 58652
Source: Proceedings - Electronic Components and Technology Conference 2001. p 564-570 (IEEE cat n 01CH37220)
Publication Year: 2001
CODEN: PECCA7 ISSN: 0569-5503
Language: English
Abstract: A family of advanced thermal interface materials for high-power flip-chip **BGA** form factor (FCBGA) **packages** is described. These silver-filled adhesives provide for high reliability on laminate FCBGA **packages**. The development of these materials are expected to enable the next level of performance, both in terms of thermal dissipation and **package** reliability. (Edited abstract) 25 Refs.

25/3,AB/9 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05693374
E.I. No: EIP00115384599
Title: **Heat spreading** resistance model for anisotropic thermal conductivity materials in electronic **packaging**
Author: Ying, T.M.; Toh, K.C.
Corporate Source: Nanyang Technological Univ, Singapore
Conference Title: 7th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems-ITherm 2000
Conference Location: Las Vegas, NV, USA Conference Date: 20000523-20000526
E.I. Conference No.: 57476
Source: Thermomechanical Phenomena in Electronic Systems -Proceedings of the Intersociety Conference v 1 2000. p 314-321
Publication Year: 2000
CODEN: PITEFT
Language: English
Abstract: The electronic **package** structure often comprises of materials that occur in thin layers. In many instances, these materials are lumped together as a simplified compact model to represent their thermal performance enabling parametric studies of the **package** structure. This new compact structure will have a new set of thermal properties that differs from its constituent components. Their combined material properties

often display anisotropic thermal conductivity because layers of conductive and less conductive materials results in an orthogonal heat transfer behavior. This paper addresses the analytical and numerical studies of **heat spreading** in an anisotropic conductivity material with particular reference to the printed circuit boards (PCB). The PCB is considered to be a single material with highly anisotropic thermal conductivity, depending on the distribution of **copper** planes and thermal vias. The motivation for this study is to determine an appropriate anisotropic spreading resistance formulation that can be used in compact models of electronic **packages**. (Author abstract) 11 Refs.

25/3,AB/10 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04697445
E.I. No: EIP97053658148
Title: Thermal and mechanical evaluations of a cost-effective plastic **ball grid** array **package**
Author: Chen, Kuan-Luen; Lau, John H.; Wu, Frank H.
Corporate Source: Express Packaging Systems, Inc, Palo Alto, CA, USA
Conference Title: Proceedings of the NEPCON WEST'97. Part 2 (of 3)
Conference Location: Anaheim, CA, USA Conference Date: 19970223-19970227
E.I. Conference No.: 46379
Source: National Electronic Packaging and Production Conference-Proceedings of the Technical Program (West and East) v 2 1997. Reed Exhibition Companies, Norwalk, CT, USA. p 1042-1054
Publication Year: 1997
CODEN: NEPPAL ISSN: 0470-0155
Language: English
Abstract: The temperature **distribution** and **thermal** resistance of a face-down **PBGA** (Plastic **Ball Grid** Array) **package** assembled on a FR-4 epoxy glass PCB (Printed Circuit Board) are presented. By varying the thickness of the **copper heat spreader** and organic substrate, an optimum **PBGA package** is designed. The effect of power and ground planes in the PCB and the size of PCB on the thermal performance of the **PBGA** is also given. Furthermore, the warpage (deflection) of the **package** under thermal loading is predicted. (Author abstract) 5 Refs.

25/3,AB/11 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04602730
E.I. No: EIP97013496615
Title: Thermal resistance and thermal warpage of cavity-down plastic **ball grid** array **packages**
Author: Chen, Kuan-Luen; Lau, John H.; Wu, Frank H.
Corporate Source: Express Packaging Systems, Inc, Palo Alto, CA, USA
Conference Title: Proceedings of the 1996 ASME International Mechanical Engineering Congress & Exhibition
Conference Location: Atlanta, GA, USA Conference Date: 19961117-19961122

E.I. Conference No.: 45867
Source: American Society of Mechanical Engineers (Paper) 1996. ASME, New York, NY, USA. 9p
Publication Year: 1996
CODEN: ASMSA4 ISSN: 0402-1215
Language: English
Abstract: The temperature **distribution** and **thermal** resistance of a face-down **PBGA** (Plastic **Ball Grid** Array) **package** assembled on a FR-4 epoxy glass PCB (Printed Circuit Board) are presented. By varying the thickness of the **copper heat spreader** and organic substrate, an optimum **PBGA package** is designed. The effect of power and ground planes in the PCB and the size of PCB on the thermal performance of the **PBGA** is also given. Furthermore, the warpage (deflection) of the **package** under thermal loading is predicted. (Author abstract) 5 Refs.

25/3,AB/12 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

10553018 Genuine Article#: 540ZU Number of References: 28
Title: Thermal stress analysis of thermally-enhanced plastic **ball grid** array electronic **packaging** (ABSTRACT AVAILABLE)
Author(s): Yeh MK (REPRINT) ; Chiang KN; Su JA
Corporate Source: Natl Tsing Hua Univ,Dept Power Mech Engn,Hsinchu 30013//Taiwan/ (REPRINT); Natl Tsing Hua Univ,Dept Power Mech Engn,Hsinchu 30013//Taiwan/
Journal: CHINESE JOURNAL OF MECHANICS-SERIES A, 2002, V18, N1 (MAR), P9-16
ISSN: 1017-4370 Publication date: 20020300
Publisher: SOC THEORETICAL APPLIED MECHANICS, R O C, NATIONAL TAIWAN UNIV, TJINGLING INDUSTRIAL RES INST, TAIPEI 106, TAIWAN
Language: English Document Type: ARTICLE
Abstract: The thermally enhanced **ball grid** array (TEBGA) electronic **packaging** under thermal cycling and thermal loading was investigated numerically. Two-dimensional finite element analysis by ANSYS was used for calculating the temperature **distribution** and **thermal** stress on the symmetric and diagonal cross sections of TEBGA. The thermal failure based on the peel and shear stresses at interfaces of TEBGA took place at the interface between the heat sink and epoxy moulding compound. The Tasi-Hill failure criterion was modified to predict the failure at various interfaces in TEBGA **package**. The TEBGA geometric parameters, including the thickness of the heat sink, the thickness of the adhesive layer between the heat sink and the die, and the thickness of the reinforcing **copper** ring, were varied to assess their effects on the failure mode of TEBGA. The results showed that for a TEBGA under thermal cycling, the stress values were reduced for thicker adhesive layers and thinner heat sinks; for a TEBGA under thermal loading, the die-to-ambient thermal resistance of TEBGA decreased for thinner adhesive layers and thicker heat sinks. The slimmer heat sink of extruded plate type can dissipate more heat and can reduce the stress values. Proper choice of geometric parameters of TEBGA **package** can prevent its failure at interfaces and furthermore, improve the reliability of electronic **packaging**.

25/3,AB/13 (Item 2 from file: 34)

09025140 Genuine Article#: 358AJ Number of References: 10
Title: Quantitative analysis of pulmonary neuroendocrine cell distribution of the fetal small airways using double-labeled immunohistochemistry (ABSTRACT AVAILABLE)
Author(s): Aita K (REPRINT) ; Doi M; Tanno K; Oikawa H; Oo MT; Ohashi N; Misawa S
Corporate Source: UNIV TSUKUBA,INST COMMUNITY MED, DEPT LEGAL MED/TSUKUBA/IBARAKI 305/JAPAN/ (REPRINT); TSUKUBA MED EXAMINERS OFF,/TSUKUBA/IBARAKI/JAPAN/
Journal: FORENSIC SCIENCE INTERNATIONAL, 2000, V113, N1-3,SI (SEP 11), P 183-187
ISSN: 0379-0738 Publication date: 20000911
Publisher: ELSEVIER SCI IRELAND LTD, CUSTOMER RELATIONS MANAGER, BAY 15, SHANNON INDUSTRIAL ESTATE CO, CLARE, IRELAND
Language: English Document Type: ARTICLE
Abstract: Pulmonary neuroendocrine cells (PNECs) are supposed to play an essential role in development of fetal lung and neonatal respiratory adaptation. Some previous studies have suggested the close relation between PNECs and sudden infant death syndrome (SIDS). To investigate how PNECs **distribute** to the **thermal** bronchioli of fetal lung may be a clue to clarify this relation. Since it is difficult to distinguish bronchiole from alveolus in fetal lung, we performed double immunostaining with antibody against chromogranin a (**CGA**) and **cu**-smooth muscle actin (SMA) which can make clear distinction between them. In this study, formalin-fixed, paraffin-embedded lung tissues from 18 autopsy **cases** from 16 to 28 weeks of gestation were assessed. **CGA** immunopositive cells were counted and the length of basement membranes of terminal bronchioli was measured with computed image analyzer. Density of PNECs was expressed as the number of immunopositive cells per millimeter of basement membrane. Terminal bronchiole stained with SMA was dearly distinguished from alveolus at 16 weeks. With gestational age, **CGA** immunopositive PNECs were gradually increased in 2 folds by the 25th week. After that, their density wasn't changed significantly until termination. It is suggested that PNECs in terminal bronchiole was playing an important role in morphogenesis of alveolar ducts and alveolar sacks. (C) 2000 Elsevier Science Ireland Ltd. All rights reserved.

27/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5950894 INSPEC Abstract Number: B9808-0170J-019, C9808-7410D-029
Title: The effect of stencil printing optimization on reliability of CBGA and **PBGA** solder joints
Author(s): Li, Y.; Mahajan, R.L.; Subbarayan, G.
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Journal: Transactions of the ASME. Journal of Electronic Packaging vol.120, no.1 p.54-60
Publisher: ASME,
Publication Date: March 1998 Country of Publication: USA
CODEN: JEPAE4 ISSN: 1043-7398
SICI: 1043-7398(199803)120:1L.54:ESPO;1-R
Material Identity Number: N602-98002
U.S. Copyright Clearance Center Code: 1043-7398/98/$3.00
Language: English
Abstract: As a follow-up and conclusion to previous work in stencil printing process modeling and optimization (Li et **al** , ASME J. Electron **Packaging** vol. 118, pp. 1-6, 1996), we investigate the effect of stencil printing optimization on the reliability of ceramic and plastic **ball grid** arrays. For ceramic **ball grid** arrays, the eutectic solder fillet shape is calculated using a series of simple mathematical equations. The **thermal** strain **distributions** within the solder joints after two cycles of accelerated thermal cycling test are estimated using three-dimensional finite element models. The modified Coffin-Manson relationship is applied to calculate the mean fatigue lives of the solder joints. The results reveal that an optimized stencil printing process significantly reduces variation in the fatigue life of ceramic **ball grid** arrays. The results also show that the fatigue life of ceramic **ball grid** arrays is very sensitive to the card-side solder volume. The maximum strain region shifts from the card-side eutectic solder to the module side as the card-side eutectic solder volume increases. This shift in maximum strain suggests that there exists an optimum ratio between the card-side solder volume and the module-side solder volume for the reliability of a given ceramic **ball grid** array design. The implications of this for the **package** developers and users are discussed. The calculations indicate that the fatigue life of plastic **ball grid** arrays is almost insensitive to the card-side solder volume.
Subfile: B C

27/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5477968 INSPEC Abstract Number: B9702-0170J-095
Title: New **BGA package** with AlN **heat-spreader**
Author(s): Okoshi, H.; Kishimoto, Y.; Kato, Y.; Okoshi, T.
Author Affiliation: Fujisawa Res. Lab., Tokuyama Corp., Kanagawa, Japan
Conference Title: Proceedings of the 9th International Microelectronics Conference p.24-7
Publisher: Microelectron. Soc, Tokyo, Japan

Publication Date: 1996 Country of Publication: Japan xv+418 pp.
Material Identity Number: XX96-01947
Conference Title: Proceedings of the 9th International Microelectronics Conference
Conference Sponsor: Microelectron. Soc.-Japan
Conference Date: 24-26 April 1996 Conference Location: Omiya, Japan
Language: English
Abstract: AlN (**aluminum** nitride) ceramics are expected to be an important **packaging** material, for their high thermal conductivity and a CTE (coefficient of thermal expansion) close to that of silicon. We have developed a cavity down **BGA** (**ball grid** array) **package** with AlN **heat-spreader** for a high performance MPU (microprocessing unit) or ASIC. This **package** was a three layer structure consisting of GND (ground), PWR (power) and SIG (signal) and was fabricated with resin adhesive. We describe the **package** structure, electrical and thermal properties and reliability testing in this paper.
Subfile: B

27/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04645435
E.I. No: EIP97033564707
Title: Effect of stencil printing optimization on reliability of CBGA and **PBGA** solder joints
Author: Li, Y.; Mahajan, R.L.; Subbarayan, G.
Corporate Source: Univ of Colorado, Boulder, CO, USA
Conference Title: Proceedings of the 1996 ASME International Mechanical Engineering Congress and Exposition
Conference Location: Atlanta, GA, USA Conference Date: 19961117-19961122
E.I. Conference No.: 45867
Source: International Symposium on Information Storage and Processing Systems American Society of Mechanical Engineers, Manufacturing Engineering Division, MED v 4 1996. ASME, New York, NY, USA. p 119-129
Publication Year: 1996
CODEN: 002548
Language: English
Abstract: As a follow-up and conclusion to previous work in stencil printing process modeling and optimization (Li et **al**., 1996), we investigate the effect of stencil printing optimization on the reliability of the ceramic and plastic **ball grid** arrays. For ceramic **ball grid** arrays, the eutectic solder fillet shape is calculated using a series of simple mathematical equations. The **thermal** strain **distributions** within the solder joints after two cycles of accelerated thermal cycling test are estimated using three-dimensional finite element models. The modified Coffin-Manson relationship is applied to calculate the mean fatigue lives of the solder joints. The results reveal that an optimized stencil printing process significantly reduces variation in the fatigue life of ceramic **ball grid** arrays. The results also show that the fatigue life of ceramic **ball grid** arrays is very sensitive to the card-side solder volume. The maximum strain region shifts from the card-side eutectic solder to the module side as the card-side eutectic solder volume increases. This

shift in maximum strain suggests that there exists an optimum ratio between the card-side solder volume and the module-side solder volume for the reliability of a given ceramic **ball grid** array design. The implications of this for the **package** developers and users are discussed. The calculations indicate that the fatigue life of plastic **ball grid** arrays is almost insensitive to the card-side solder volume. (Author abstract) 30 Refs.

27/3,AB/4 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06651123 Genuine Article#: ZH232 Number of References: 25
Title: The effect of stencil printing optimization on reliability of CBGA and **PBGA** solder joints (ABSTRACT AVAILABLE)
Author(s): Li Y (REPRINT) ; Mahajan RL; Subbarayan G
Corporate Source: UNIV COLORADO,DEPT MECH ENGN/BOULDER//CO/80309 (REPRINT)
Journal: JOURNAL OF ELECTRONIC PACKAGING, 1998, V120, N1 (MAR), P54-60
ISSN: 1043-7398 Publication date: 19980300
Publisher: ASME-AMER SOC MECHANICAL ENG, 345 E 47TH ST, NEW YORK, NY 10017
Language: English Document Type: ARTICLE
Abstract: As a follow-up and conclusion to previous work in stencil printing process modeling and optimization (Li et **al**. 1996), we investigate the effect of stencil printing optimization on the reliability of the ceramic and plastic **ball grid** arrays. For ceramic **ball grid** arrays, the eutectic solder fillet shape is calculated using a series of simple mathematical equations. The **thermal** strain **distributions** within the solder joints after two cycles of accelerated thermal cycling test are estimated using three-dimensional finite element models. The modified Coffin-Manson relationship is applied to calculate the mean fatigue lives of the solder joints. The results reveal that an optimized stencil printing process significantly reduces variation in the fatigue life of ceramic **ball grid** arrays. The results also show that the fatigue life of ceramic **ball grid** arrays is very sensitive to the card-side solder volume. The maximum strain region shifts from the card-side eutectic solder to the module side as the card-side eutectic solder volume increases. This shift in maximum strain suggests that there exists an optimum ratio between the card-side solder volume and the module-side solder volume for the reliability of a given ceramic **ball grid** array design. The implications of this for the **package** developers and users are discussed. The calculations indicate that the fatigue life of plastic **ball grid** arrays is almost insensitive to the card-side solder volume.